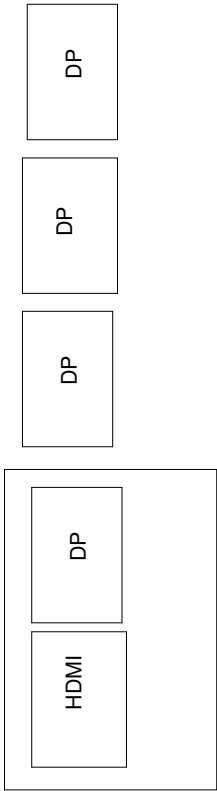


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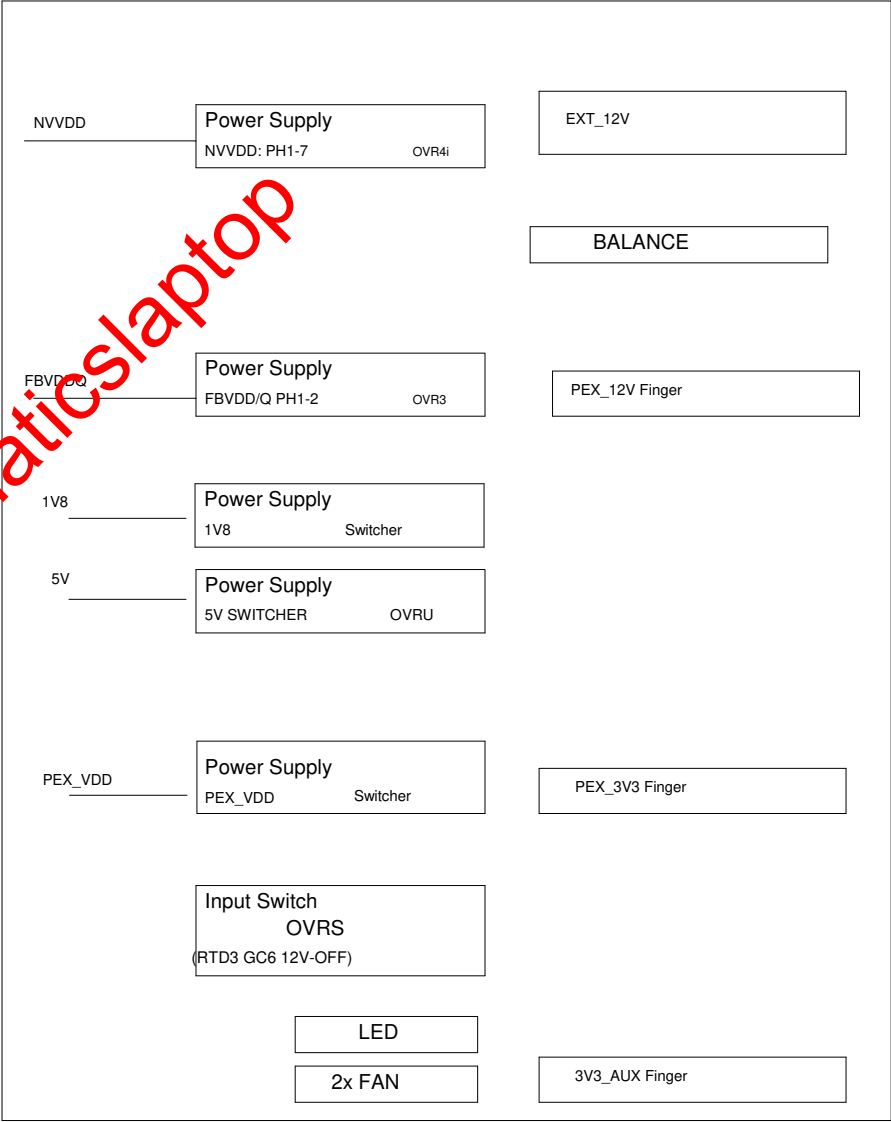
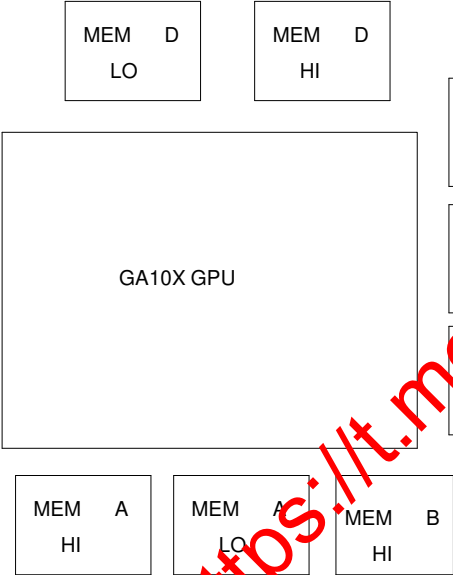
DP + DP + DP + HDMI/DP

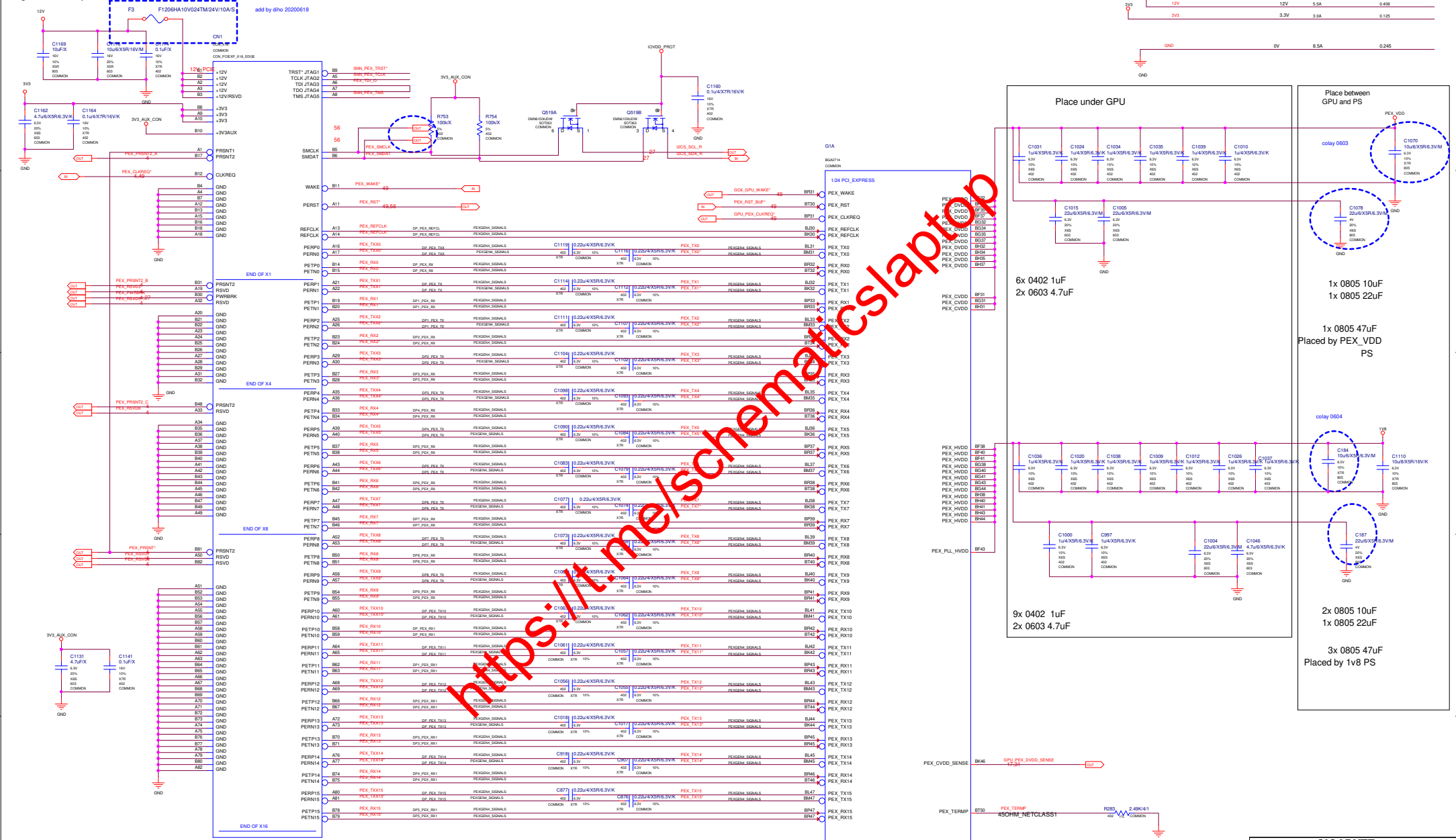
TABLE OF CONTENTS

Page	Description	Page	Description	Page	Description
1	Table of Contents	26	MISC1: ROM, XTAL,STRAPS	51	FAN & LED
2	Block Diagram	27	MISC2: JTAG,GPIO,ADC,I2C,FL,STEERO	52	PS:OVRM_PWR_SENSE
3	PCI Express	28	MISC3: RGB	53	MECH
4	PCIE GEN4 RC TERMINATIONS	29	PS: 1V8	54	PTC
5	MEMORY: GPU FB_AB	30	PS: 5V		
6	MEMORY: FBA[31:0]	31	PS: PEXVDD		
7	MEMORY: FBA[63:32]	32	PS: FBVDDQ		
8	MEMORY: FBB[31:0]	33	PS: FBVDDQ PH2		
9	MEMORY: FBB[63:32]	34	PS: NVVDD Controller		
10	MEMORY: GPU FB_CD	35	BLANK PAGE		
11	MEMORY: FBC[31:0]	36	PS: NVVDD PH4, PH6		
12	MEMORY: FBC[63:32]	37	PS: NVVDD PH1, PH3		
13	MEMORY: FBD[31:0]	38	PS: NVVDD PH2, PH5		
14	MEMORY: FBD[63:32]	39	PS: NVVDD PH9		
15	GPU PWR & GND 1	40	PS: NVVDD PH7		
16	GPU PWR & GND 2	41	PS: NVVDD PH10, PH8		
17	GPU PWR & GND 3 (XVDD)	42	PS: OVRS_INPUT POWER BALANCE		
18	GPU DECOUPLING FBVDDQ	43	PS: RDT3_12V & 9V3_Switcher		
19	GPU DECOUPLING NVVDD	44	PS: INPUTS_FILTERING and MONITORING		
20	GPU DECOUPLING NVVDD	45	PS: PEX_1V7, PEX_3V3 AND A3V3_AUX		
21	IO: IFPAB NC	46	PS: STEERING, UPB, HOT UNPLUG		
22	IO: IFPF DP	47	SEQ: 5V, 1V8, 3V3_SEQ		
23	IO: IFPE DP	48	SEQ: NVVDD, PEX, FBVDDQ ENABLE		
24	IO: IFPD DP	49	SEQ: MISC		
25	IO: IFPC HDMI/DP	50	SEQ: VOLTAGE MONITOR		



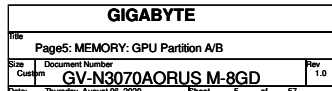
POWER SUPPLY



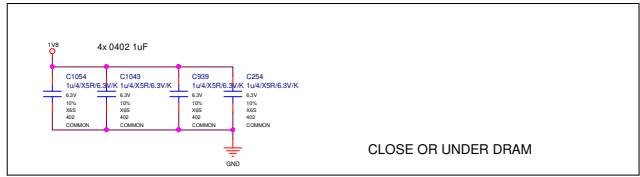
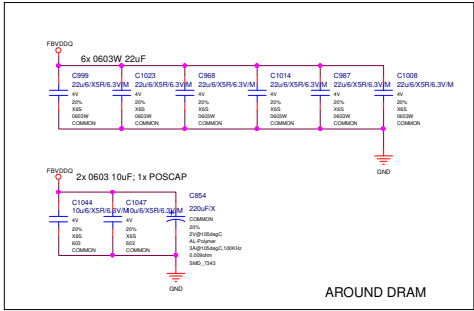
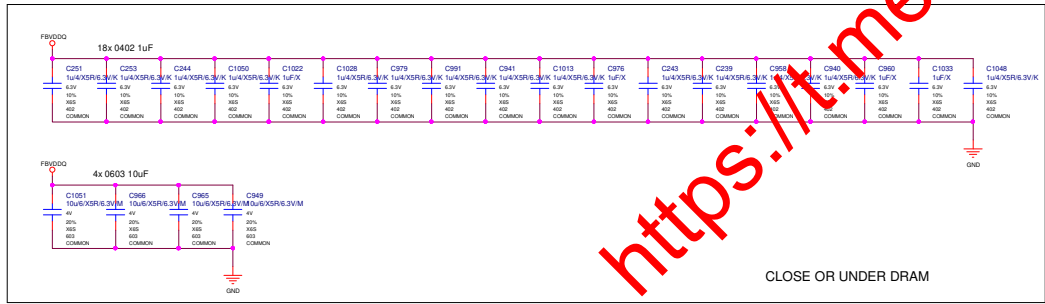
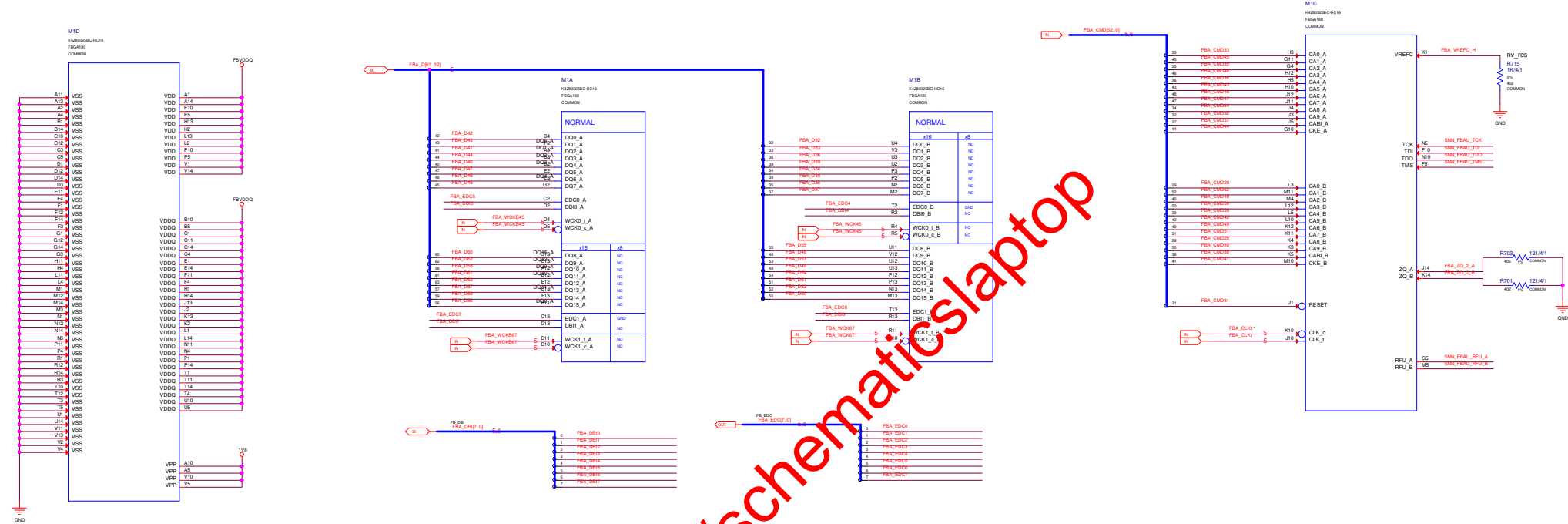


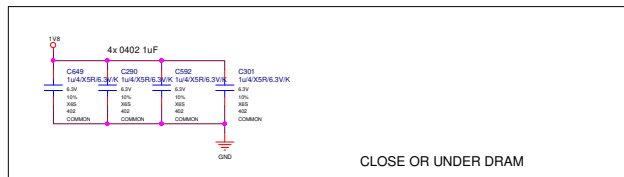
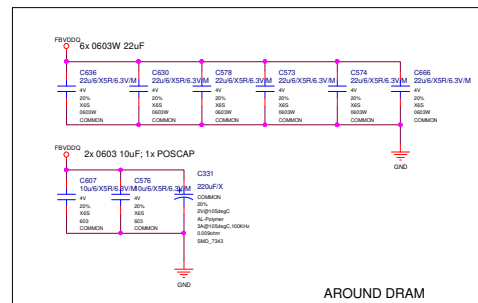
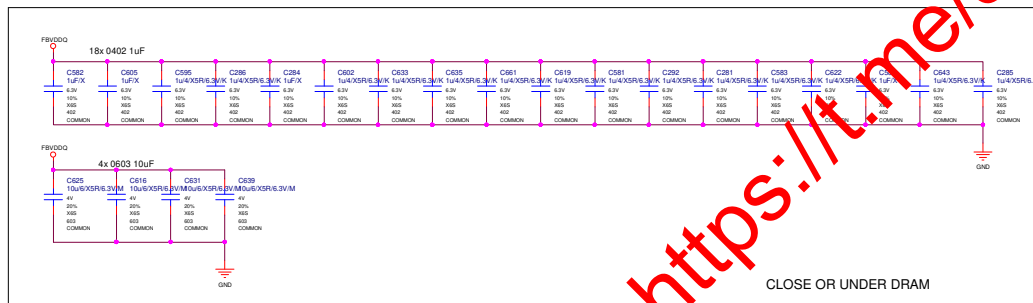
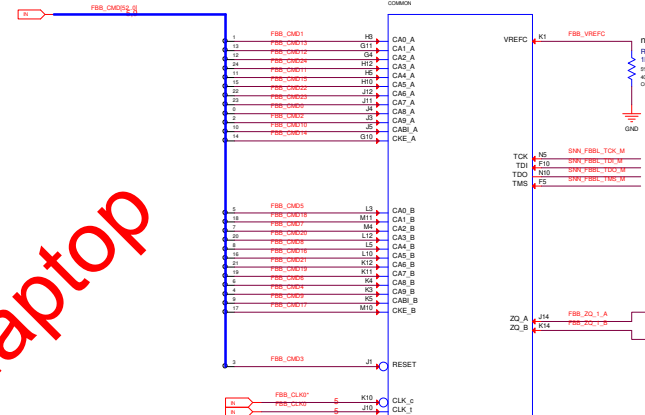
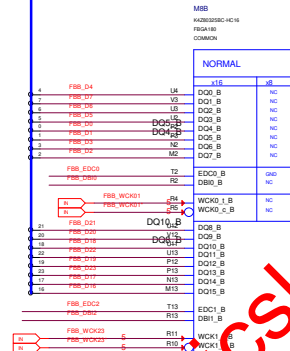
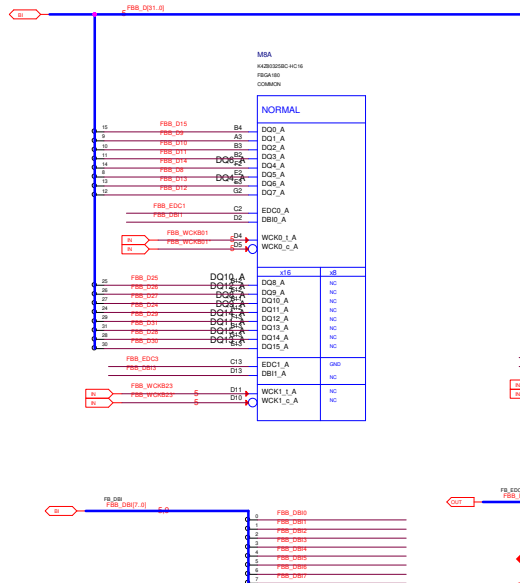


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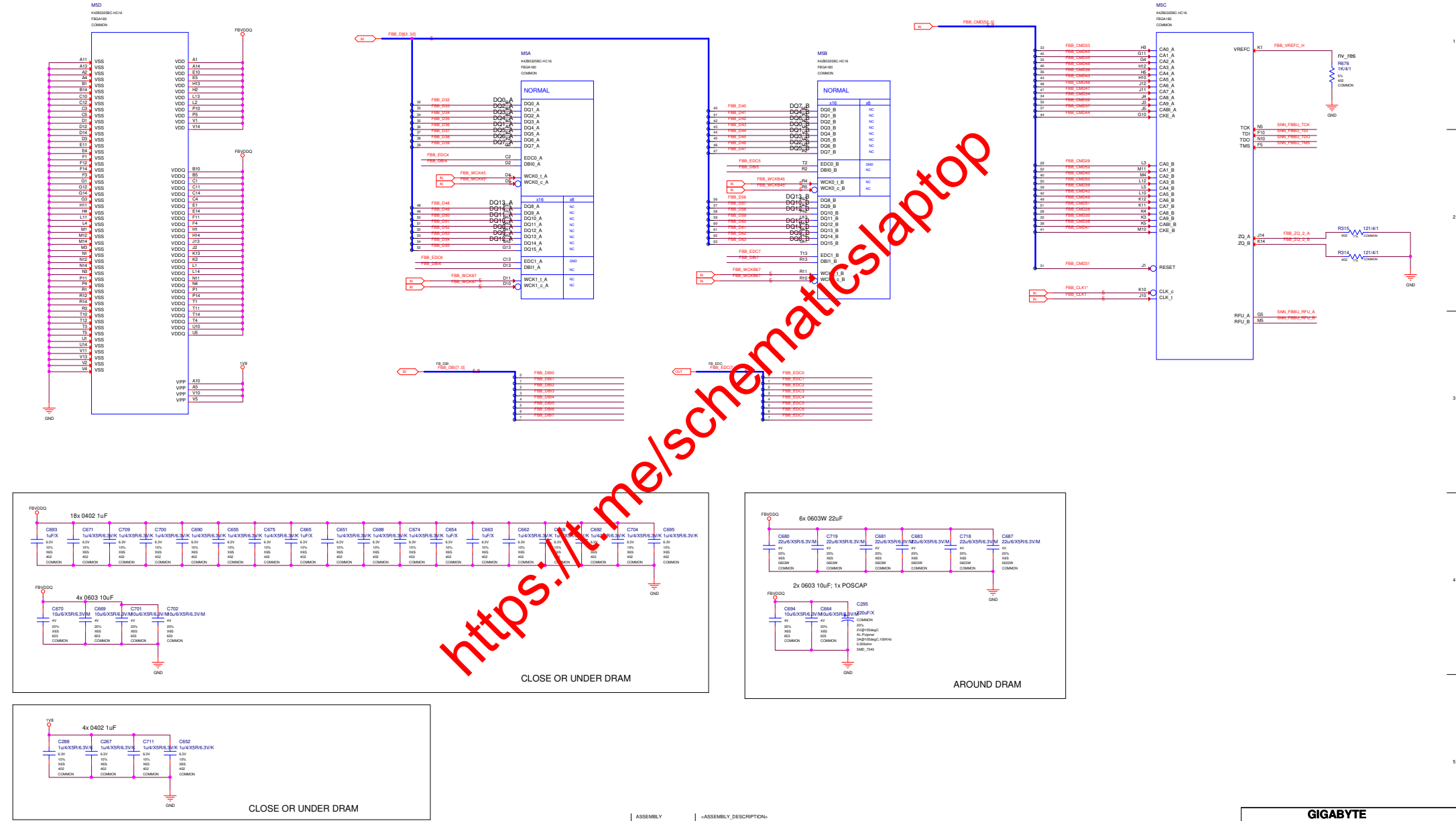




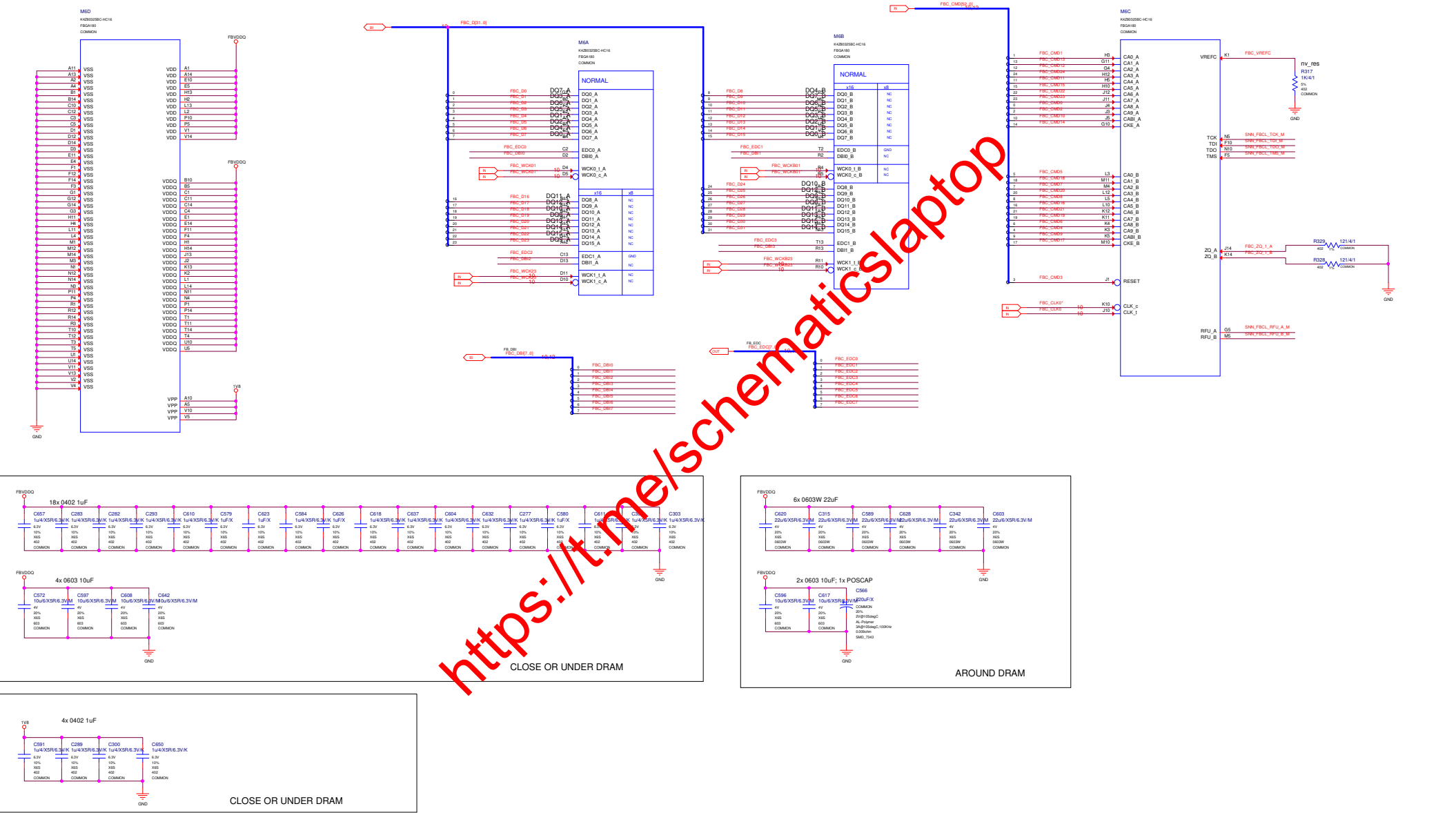


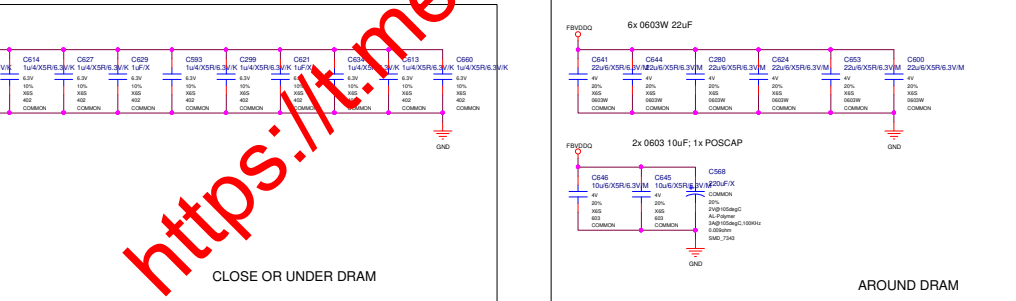
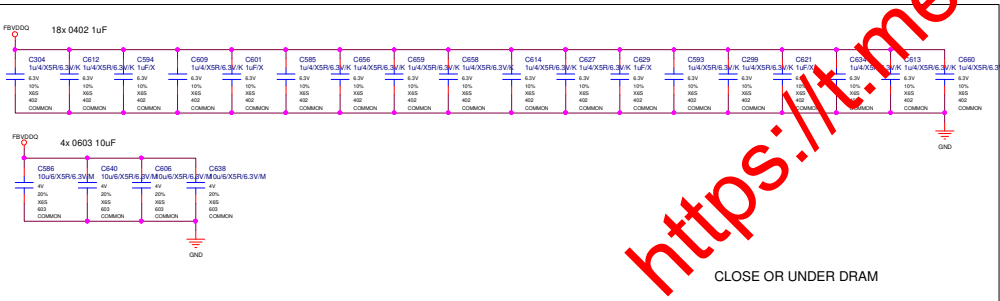


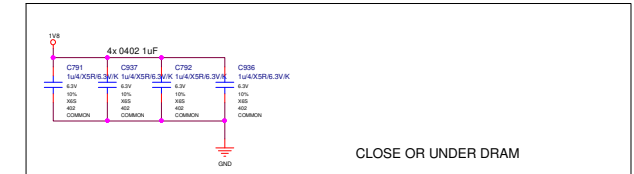
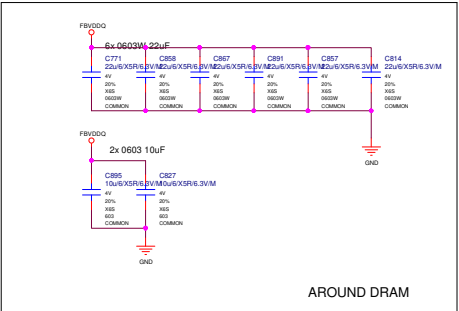
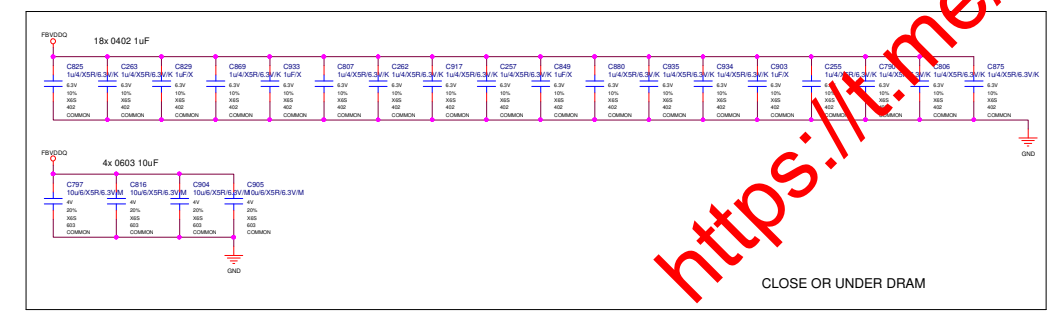
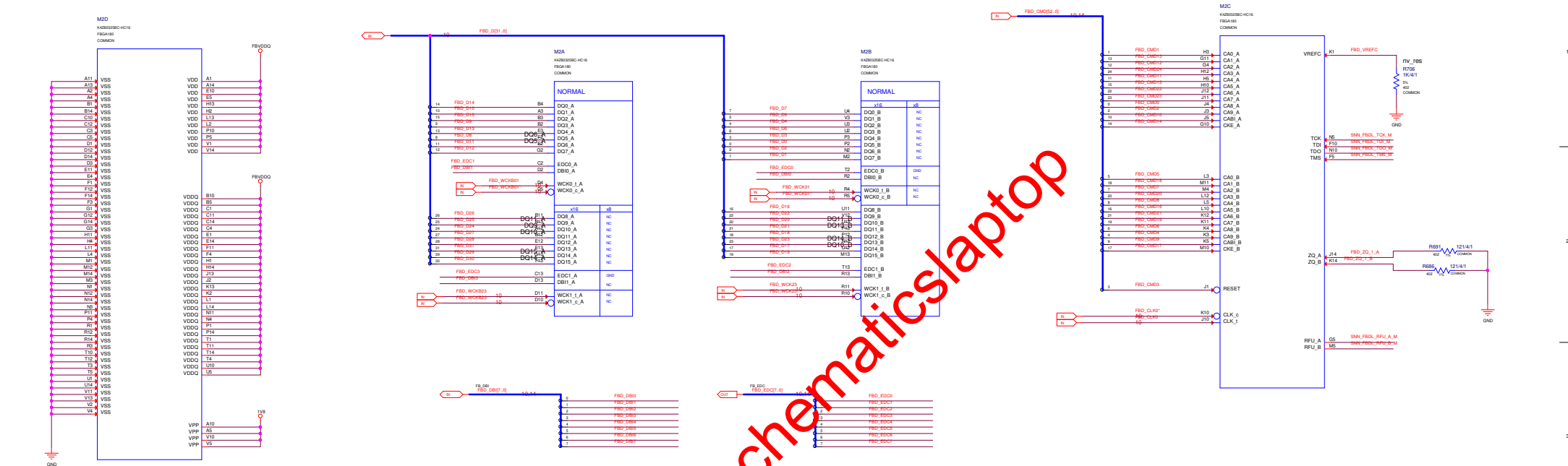


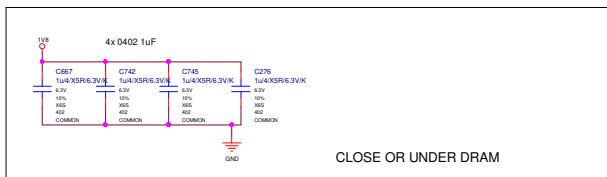
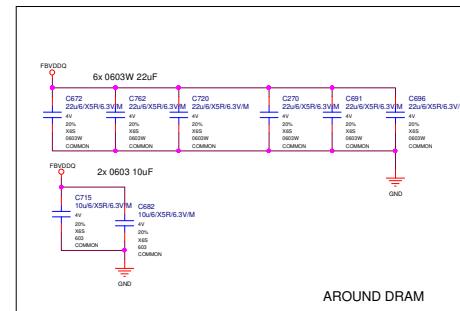
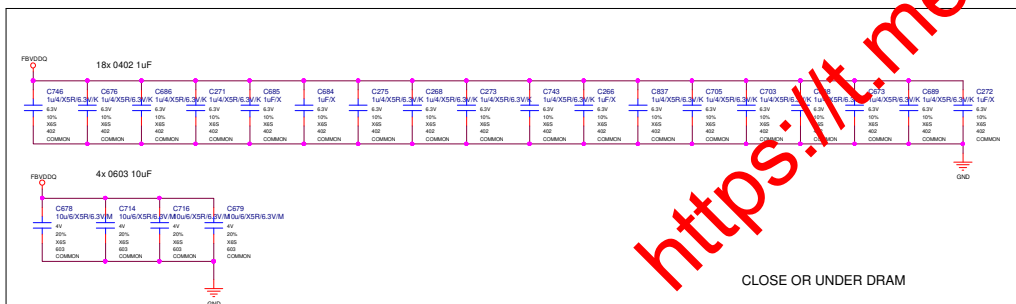
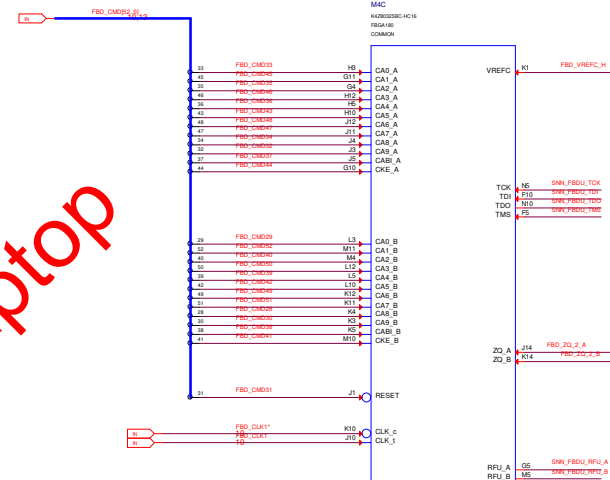
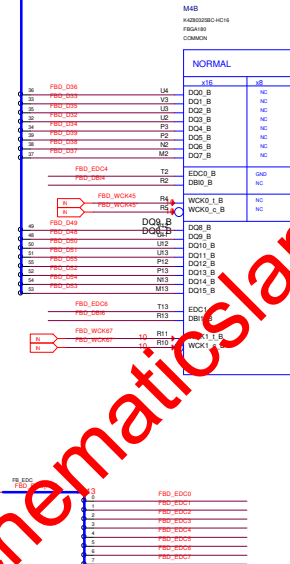
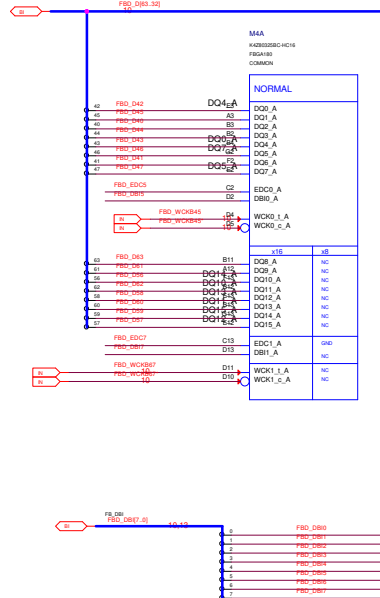


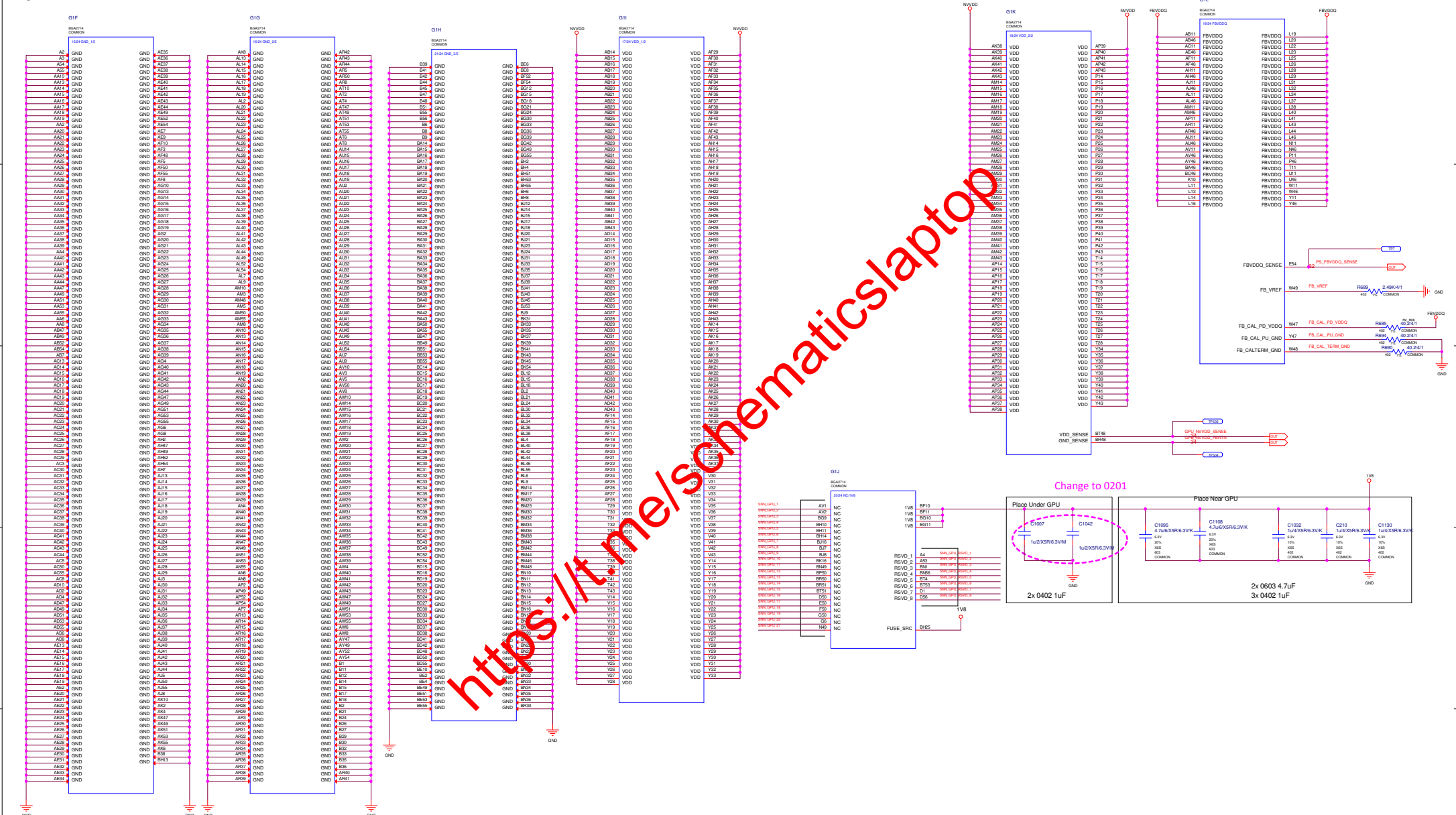


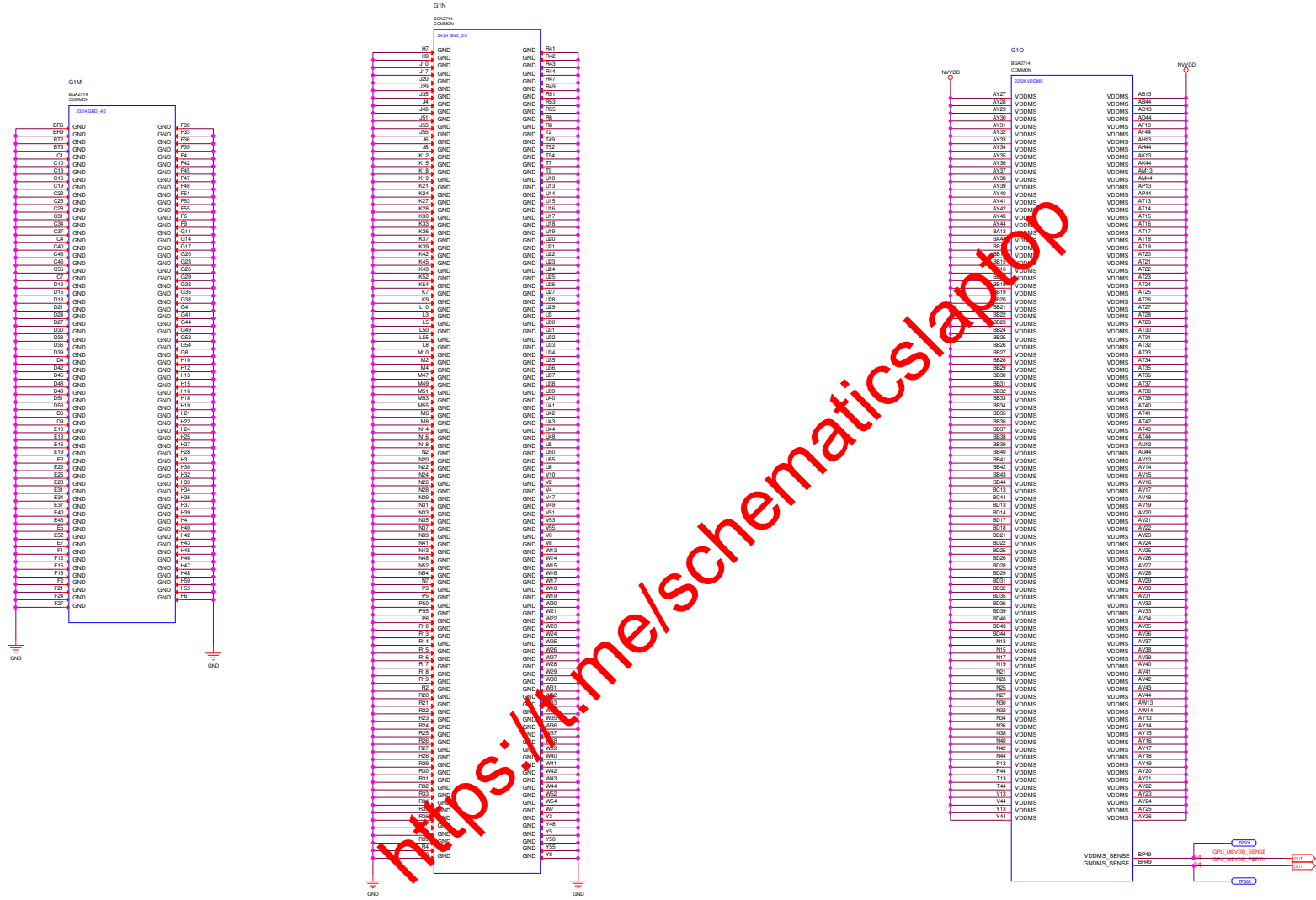




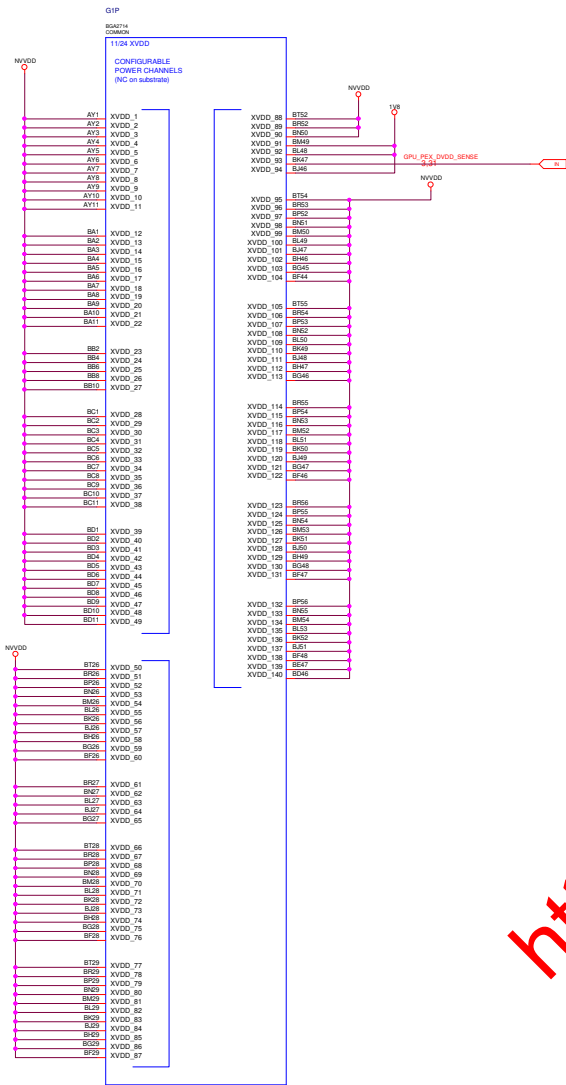






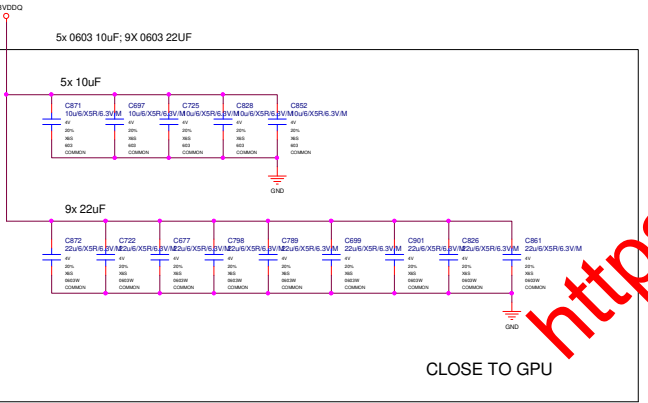
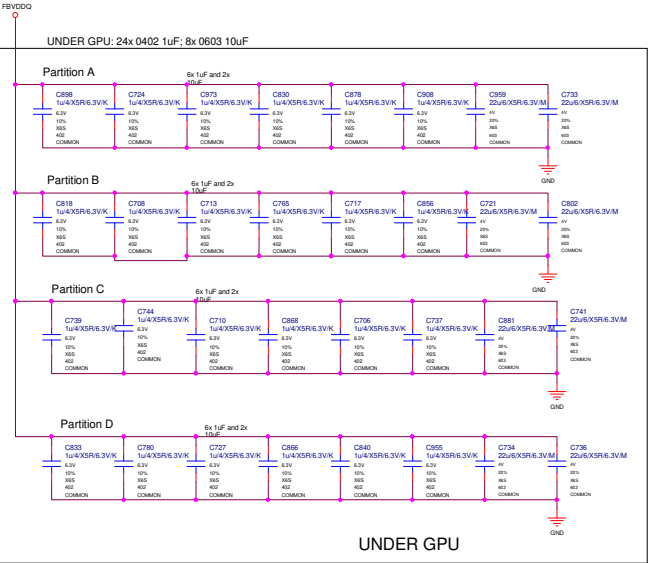






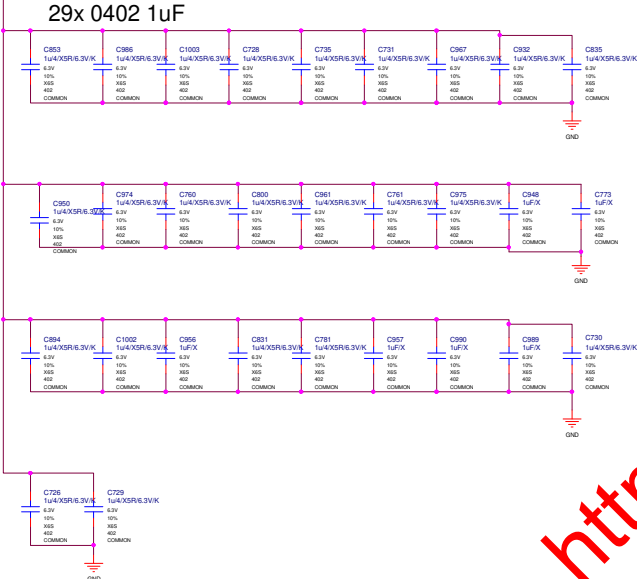
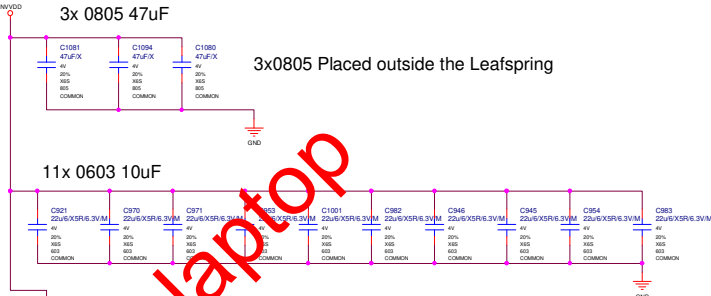
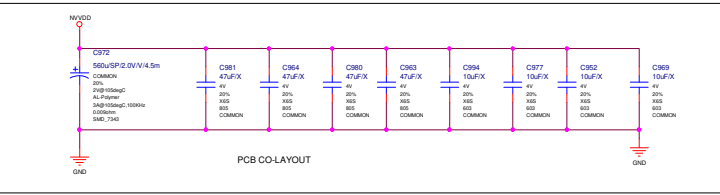
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FBVDDQ





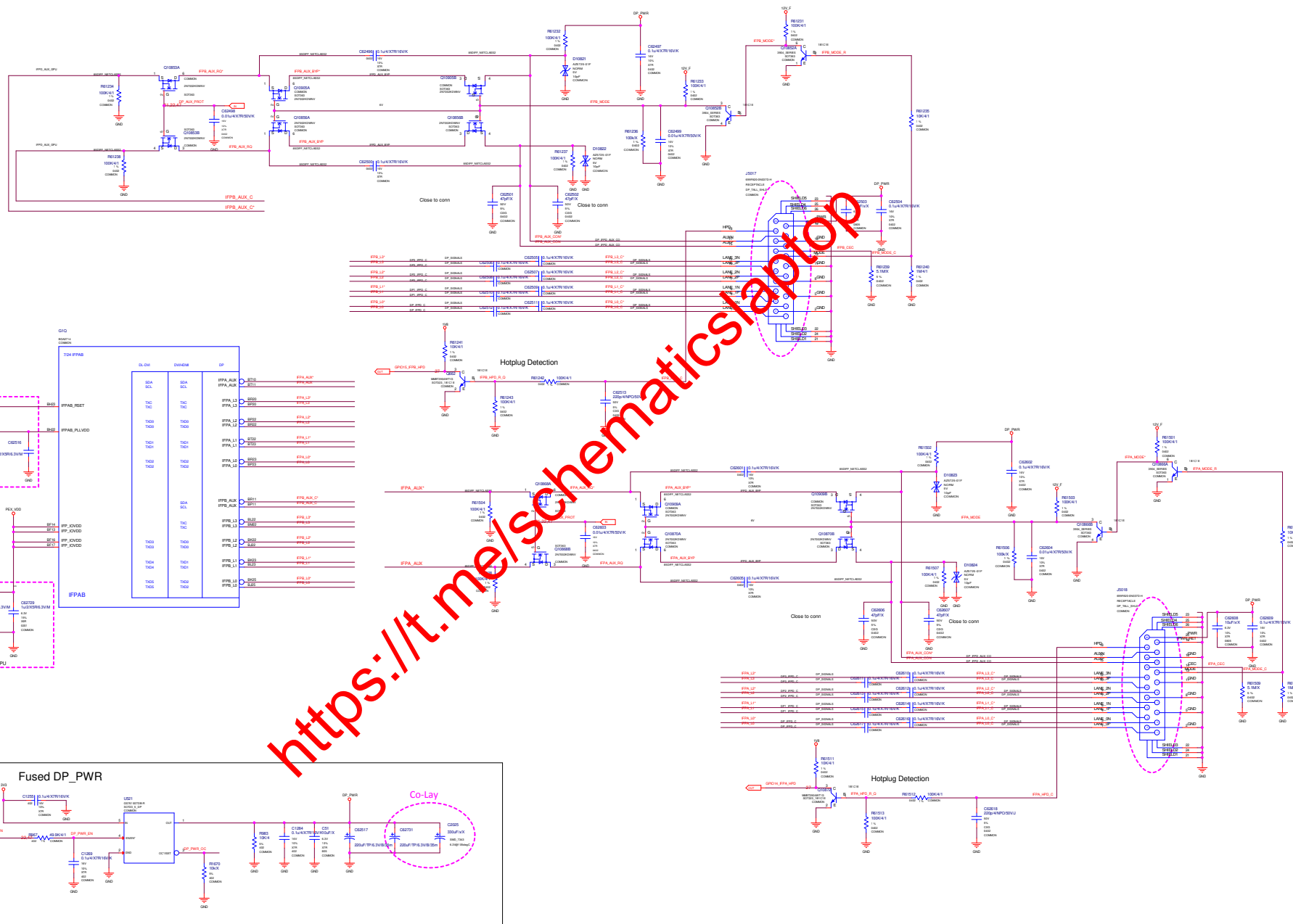
UNDER GPU



UNDER GPU

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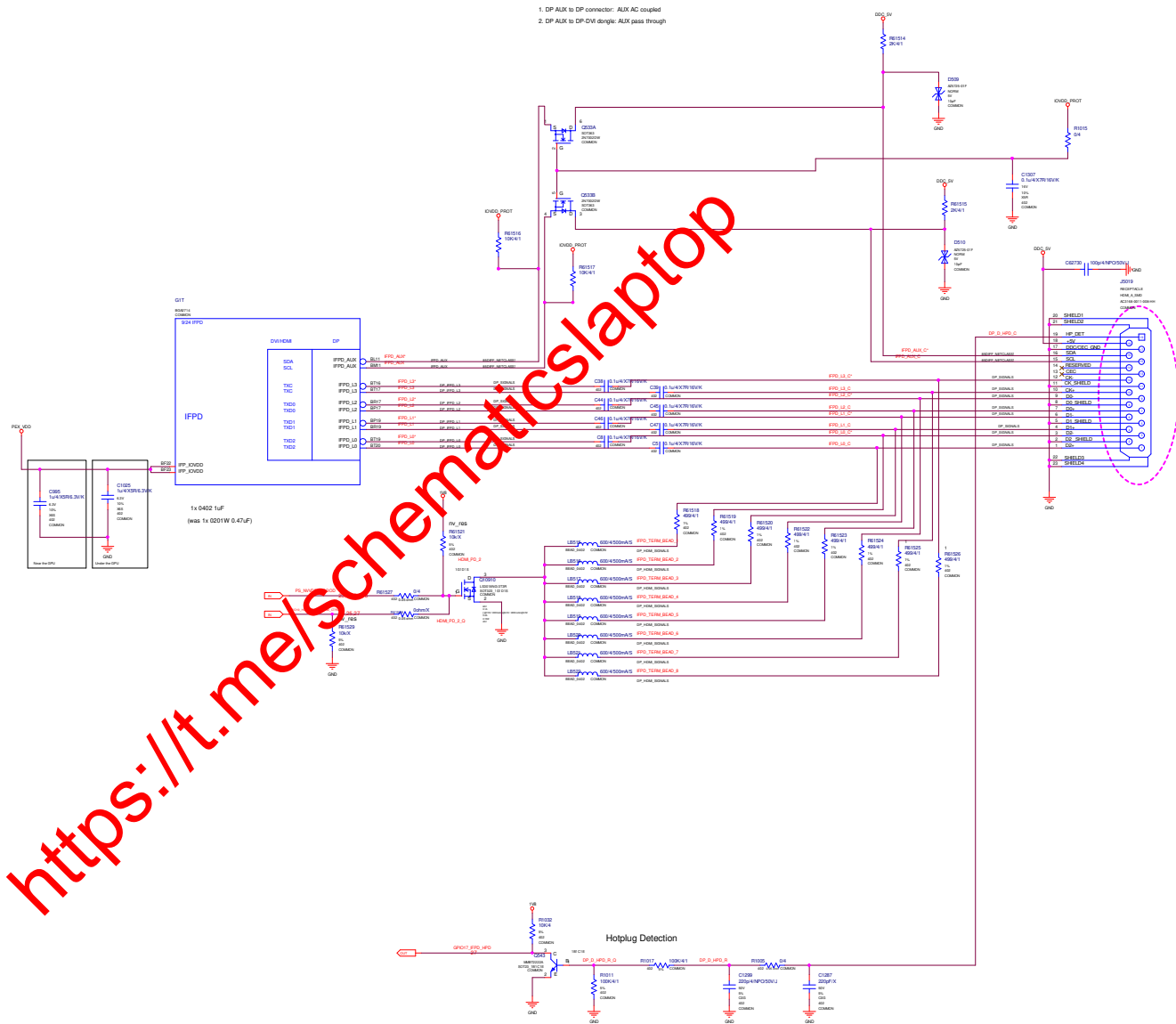
IFPA, IFPB For DP x2



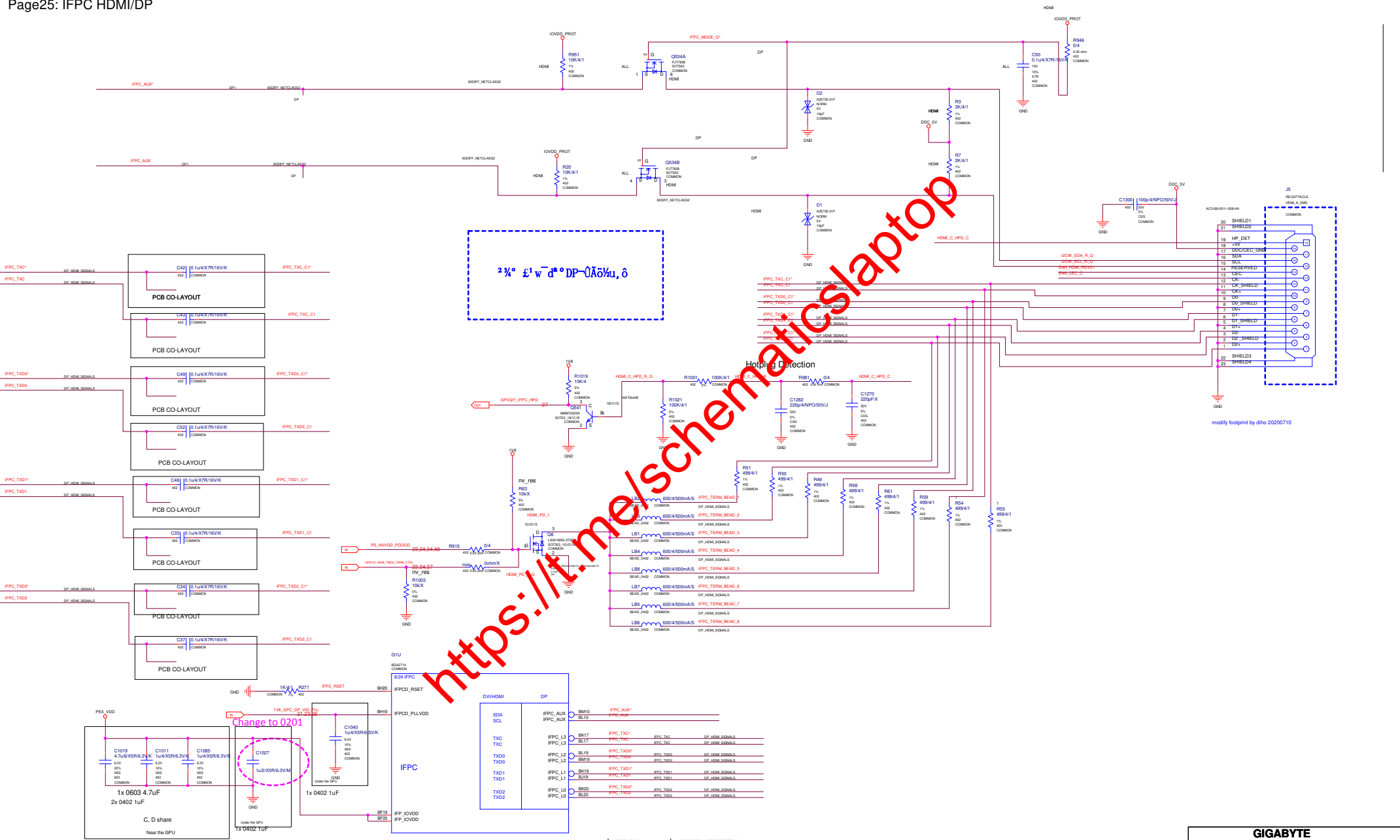




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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
TBD				

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

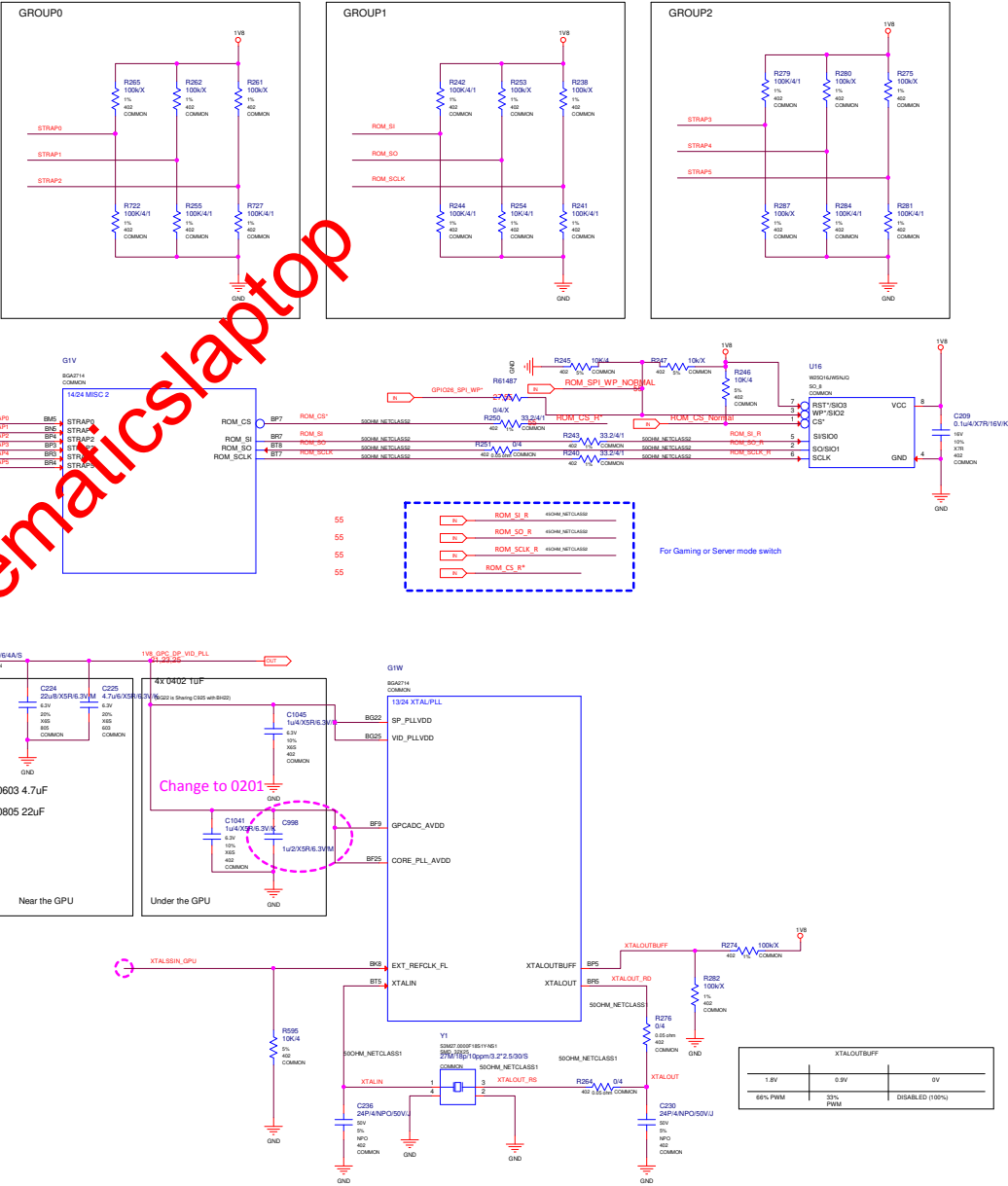
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

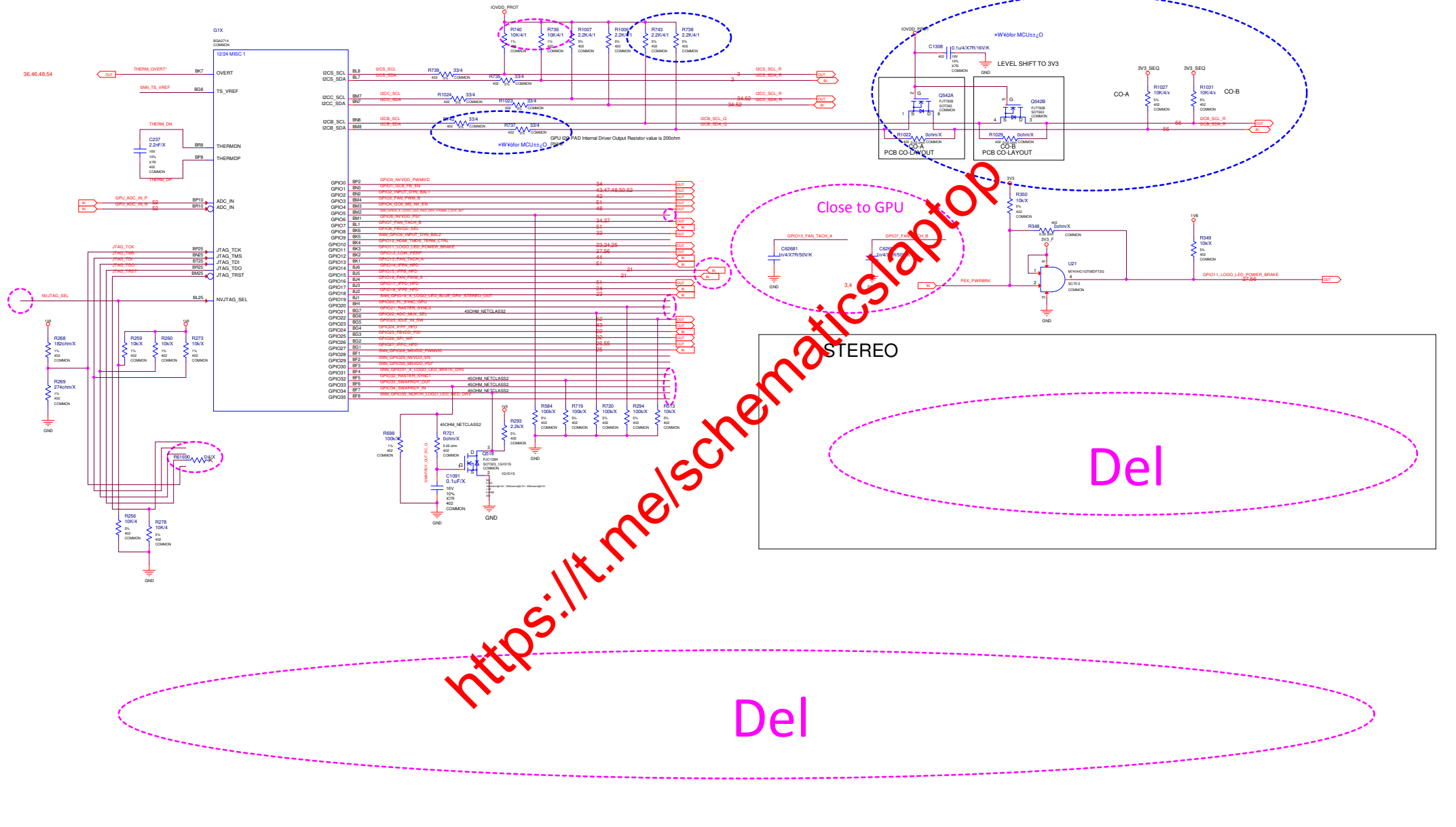
1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

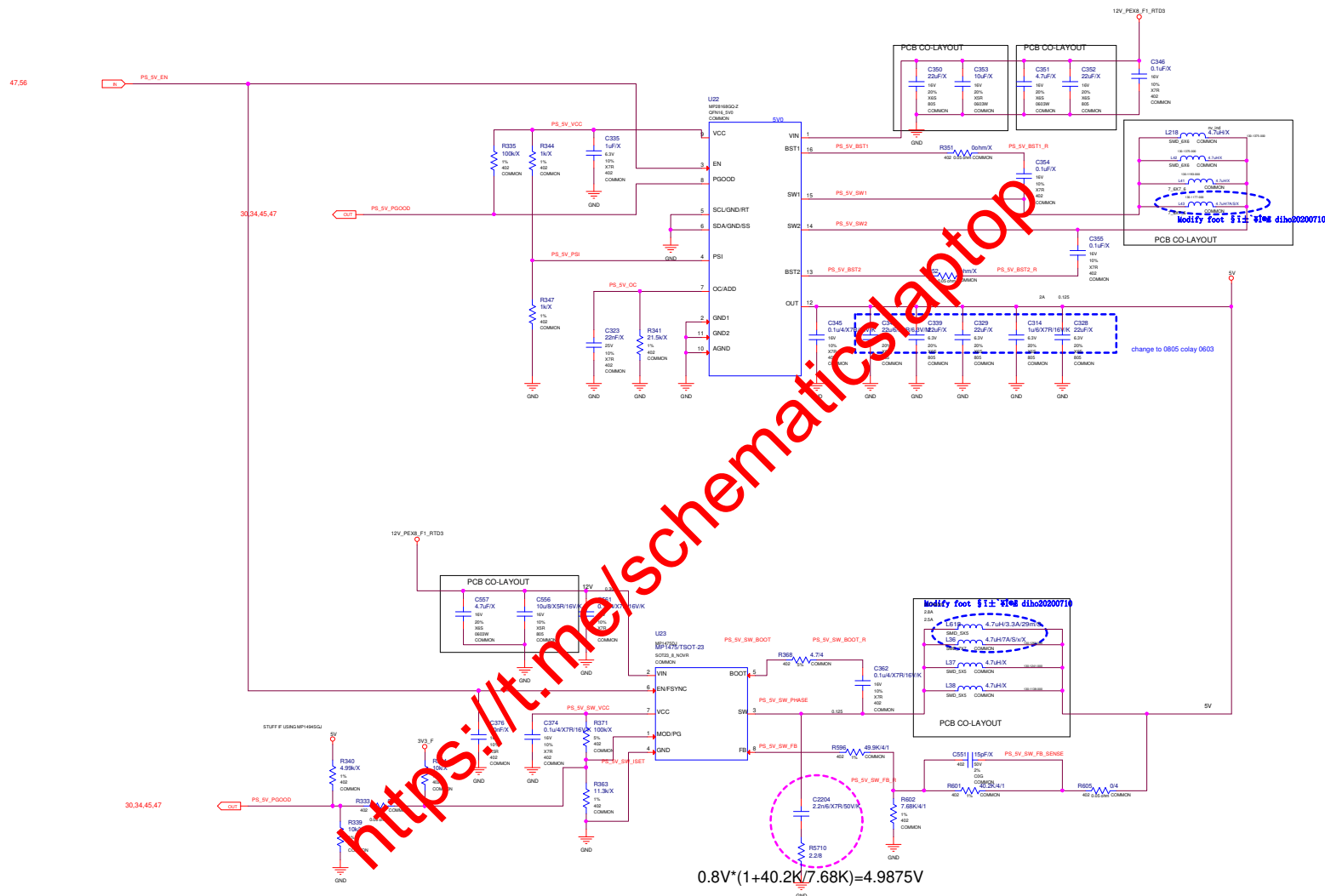
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

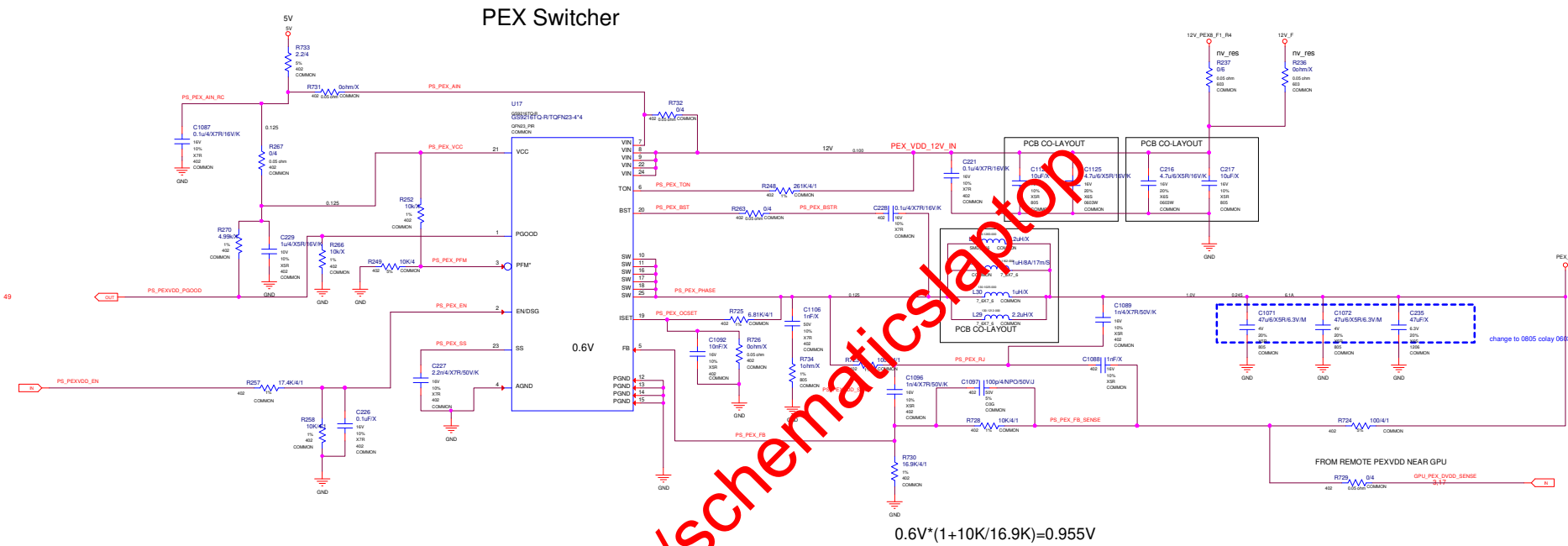




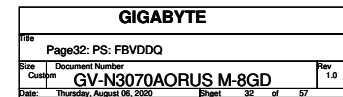






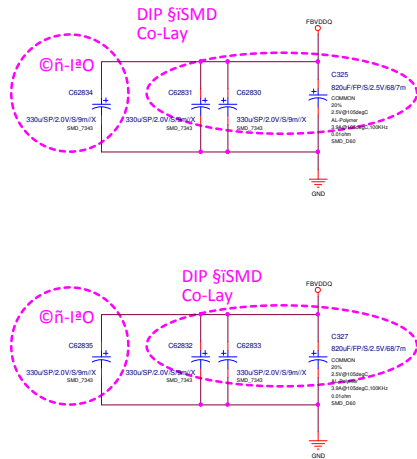
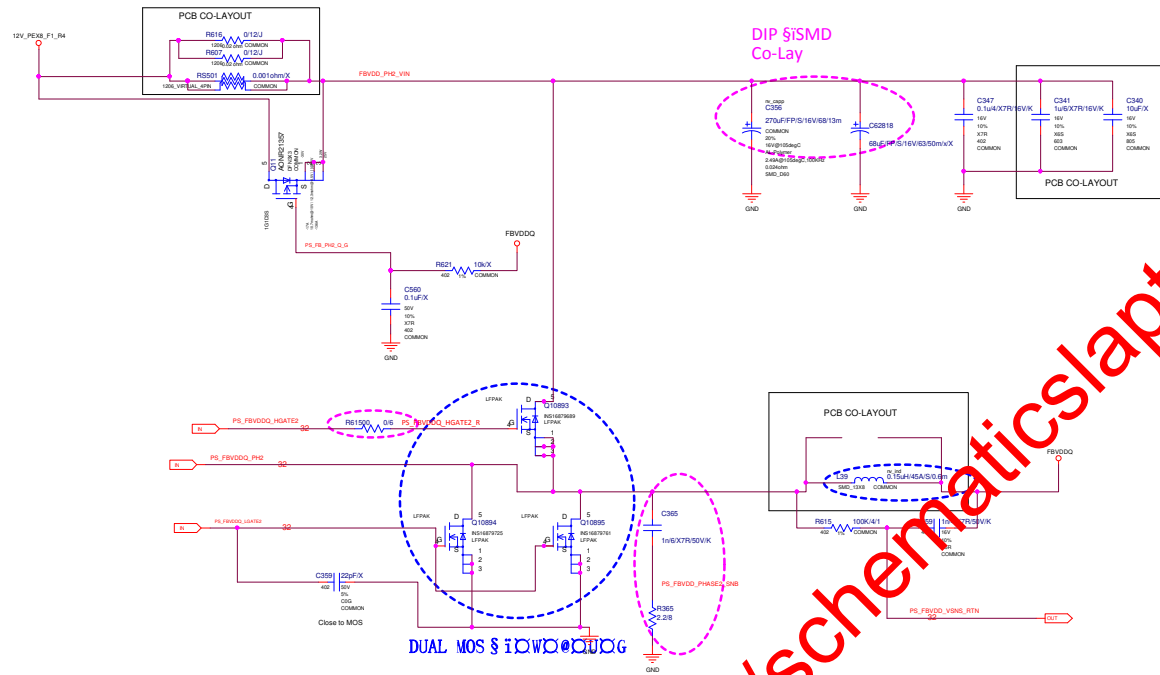


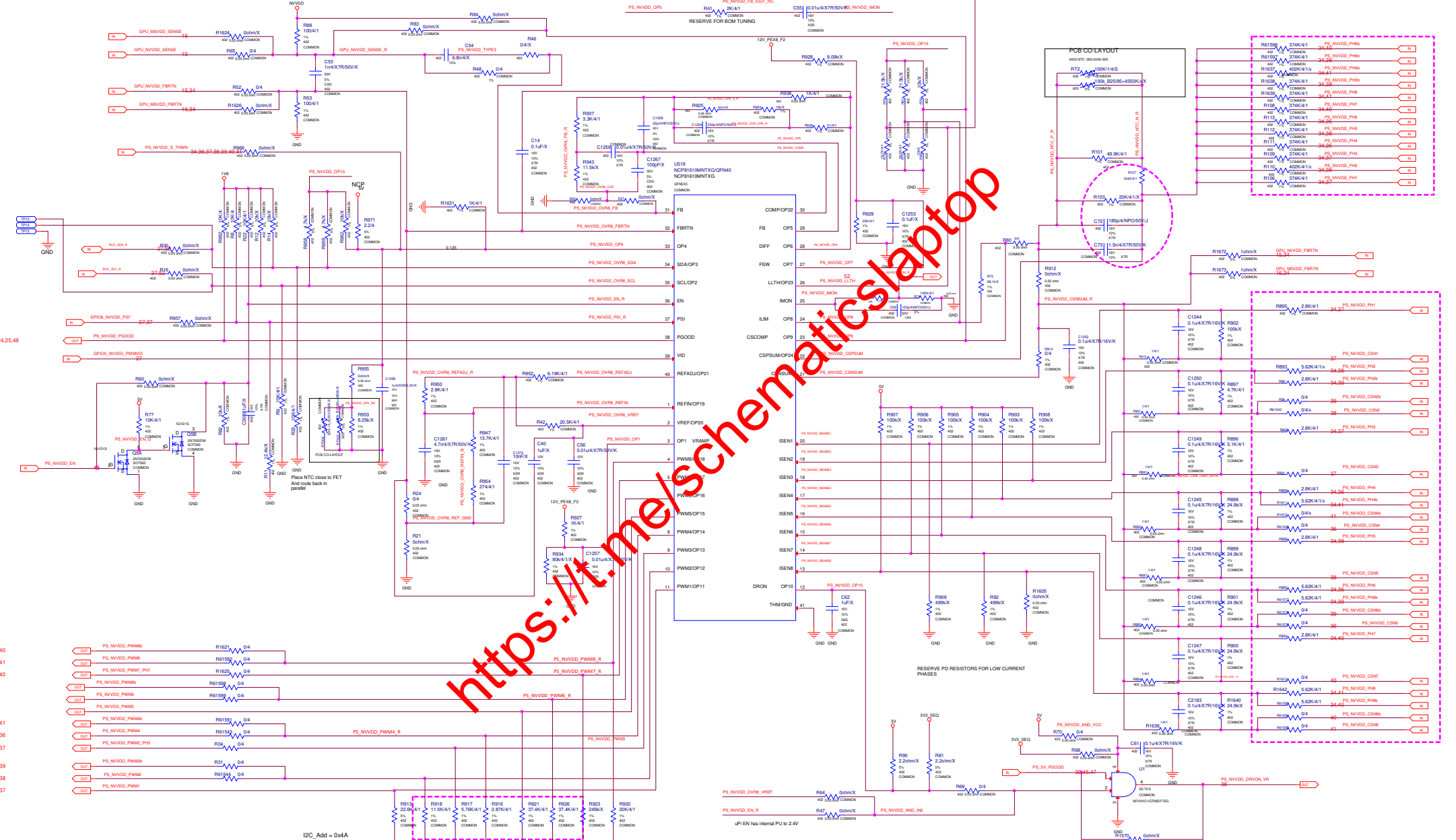
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## FBVDD PH2 INPUT ANTI-BACKDRIVE





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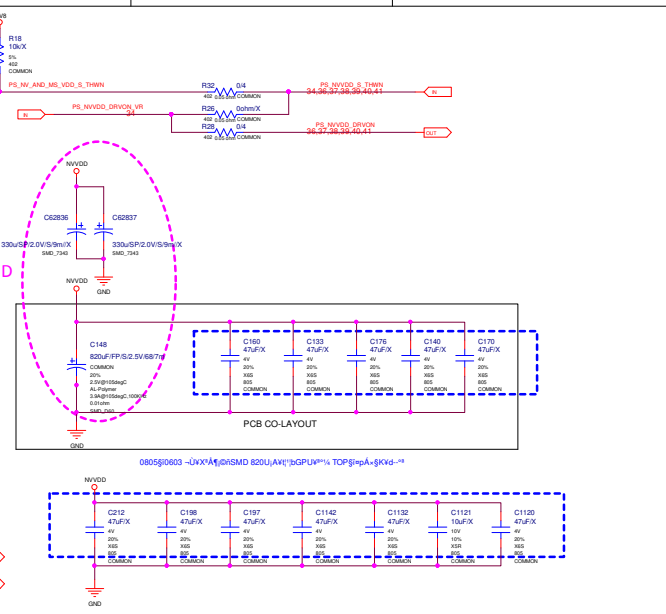
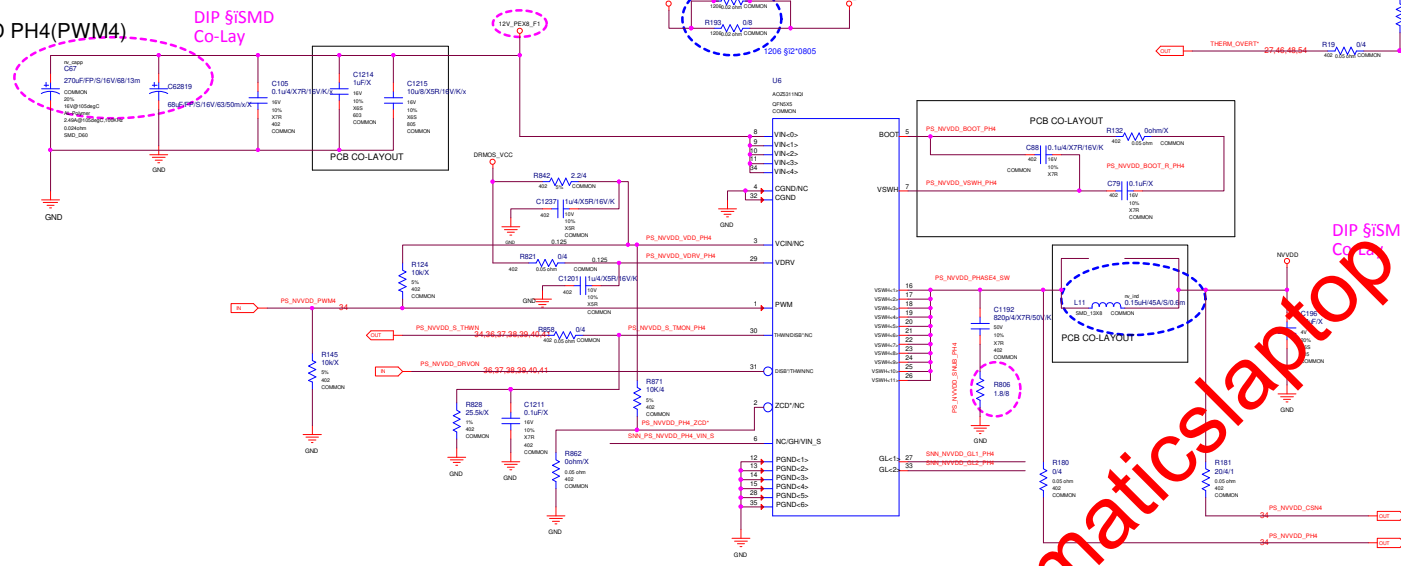
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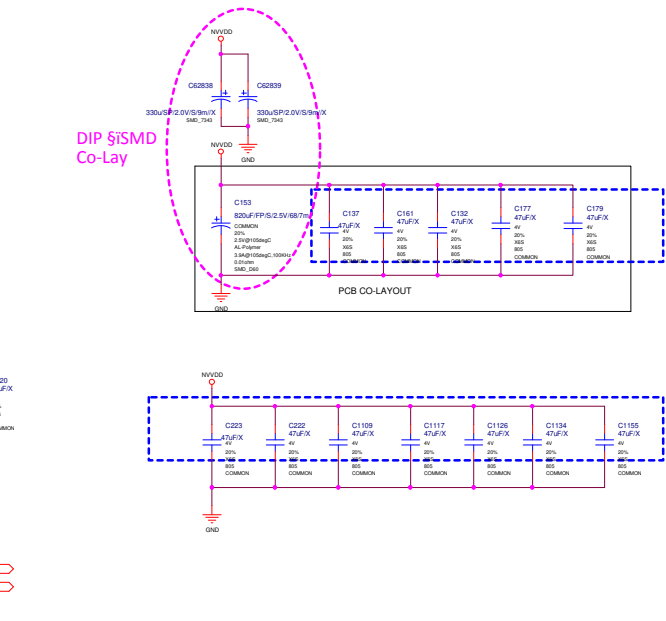
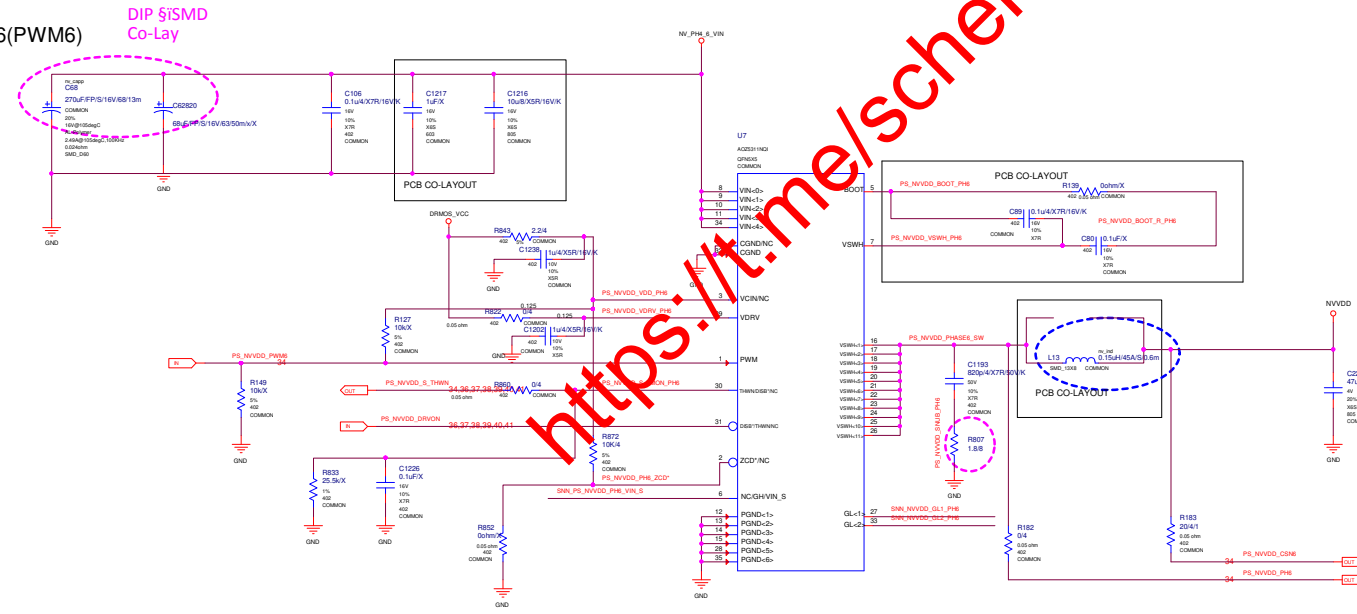
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Date Tuesday, July 21, 2020	Sheet 95	of 97

NVVDD PH4(PWM4)

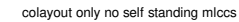


NVVDD PH6(PWM6)



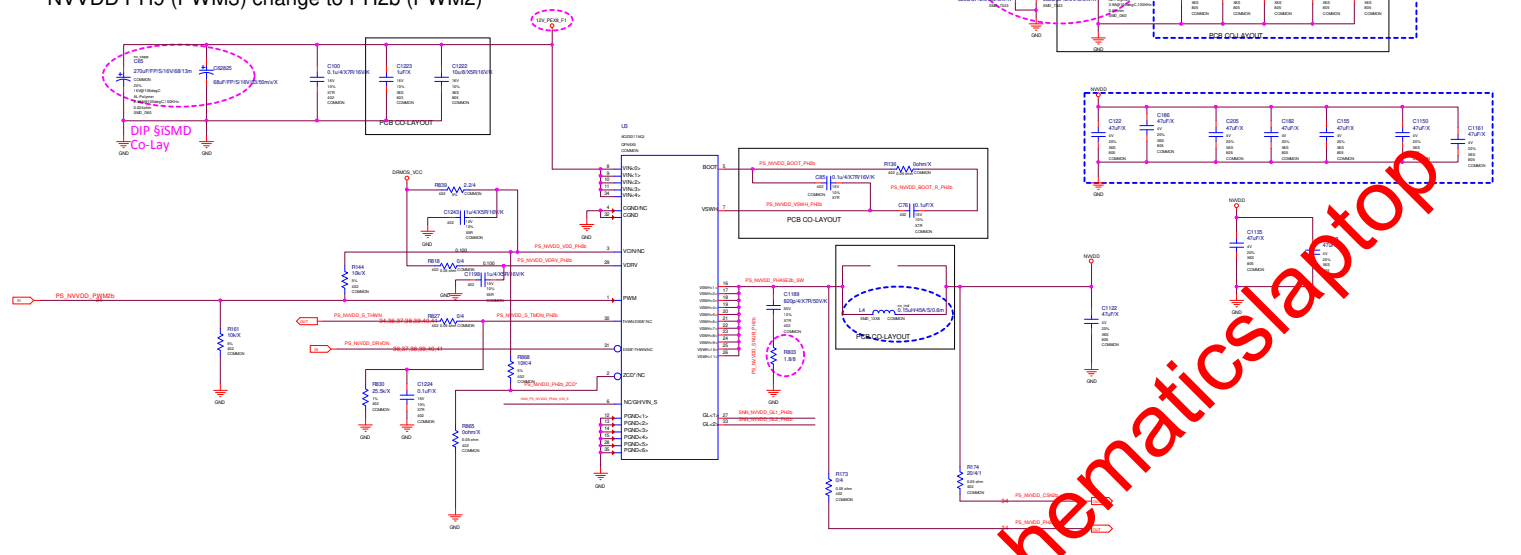


DIP ŞİSMD  
Co-Lay

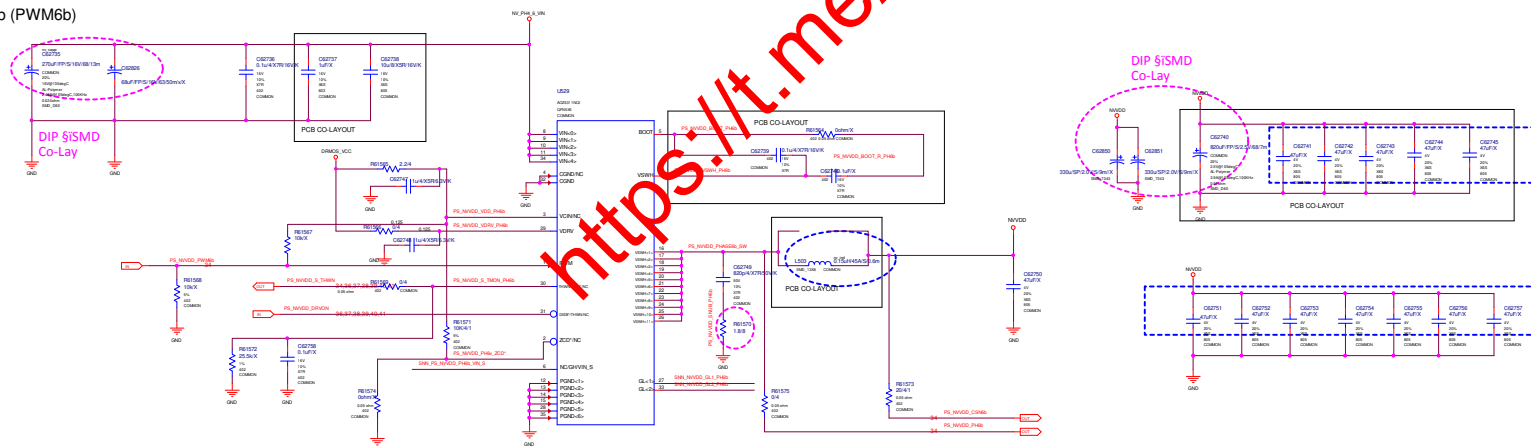




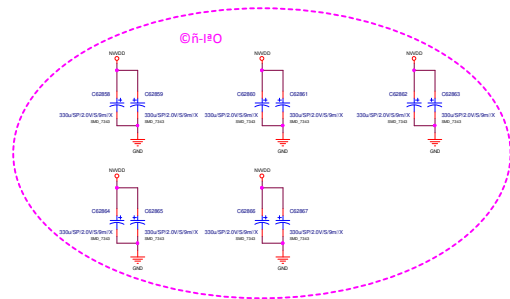
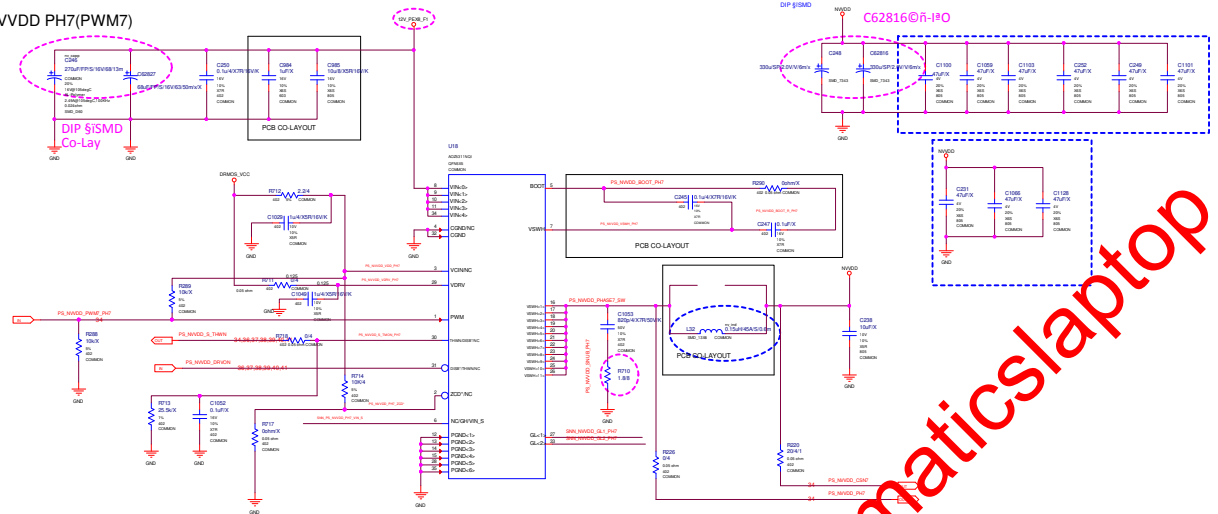
NVVDD PH9 (PWM3) change to PH2b (PWM2)



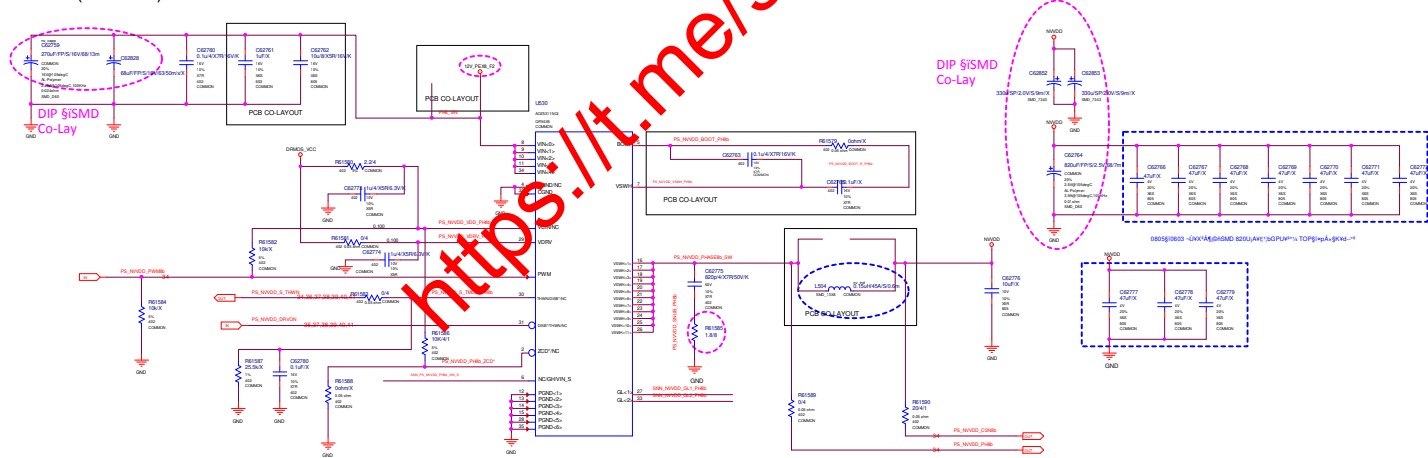
NVVDD PH6b (PWM6b)



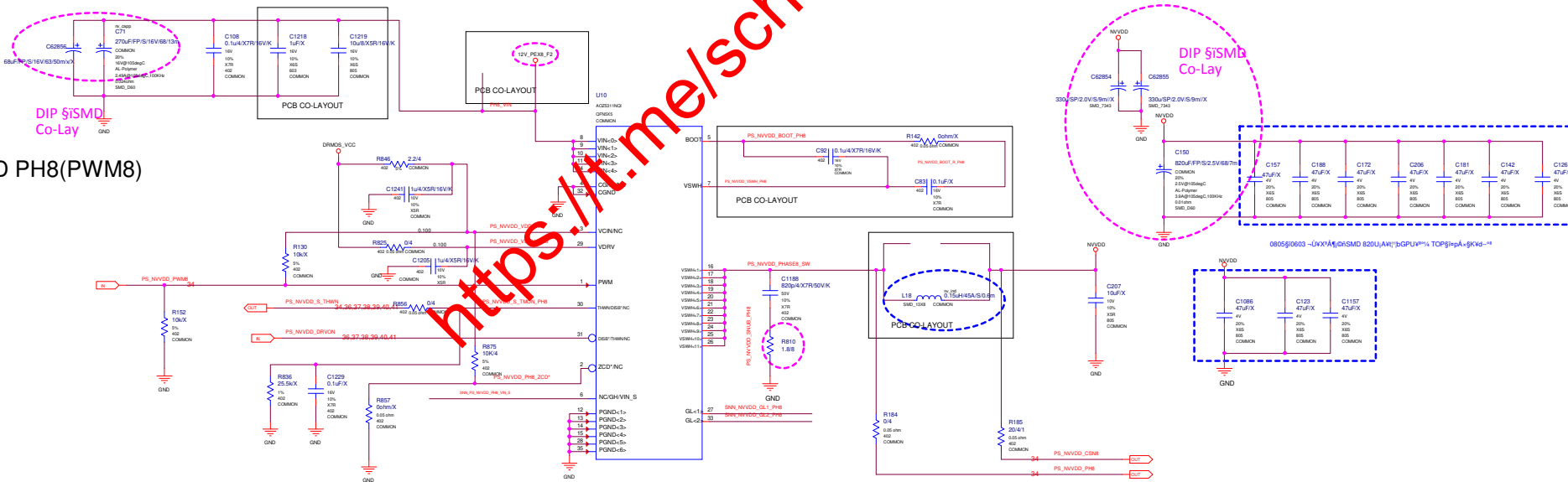
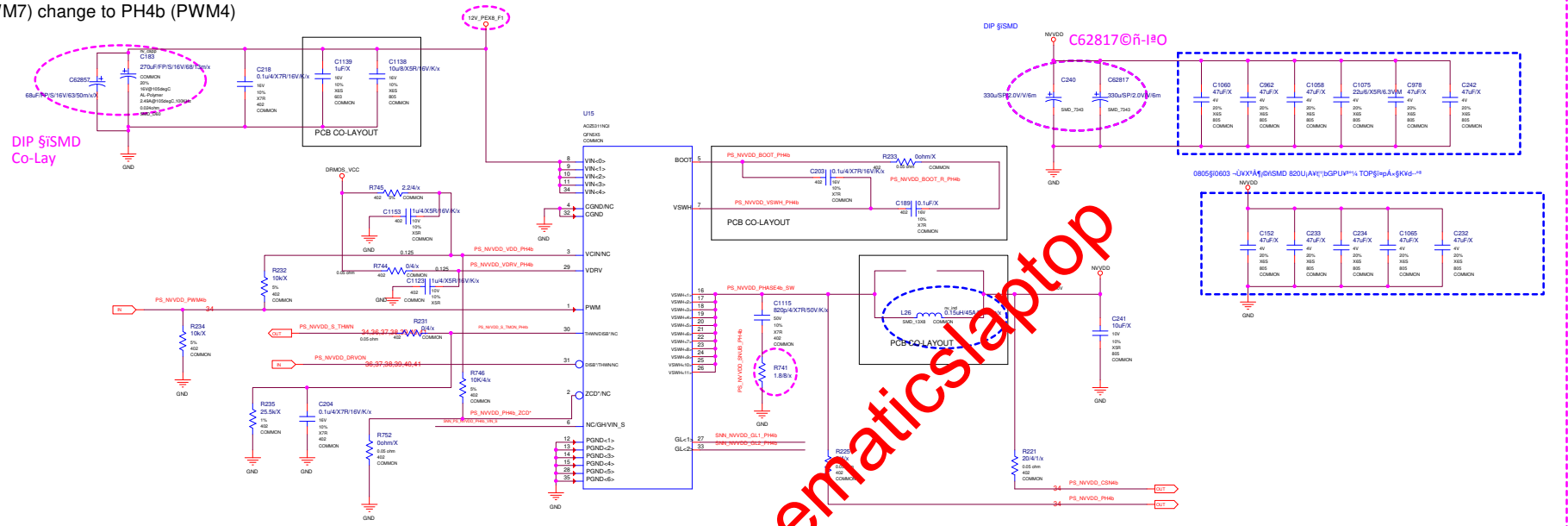
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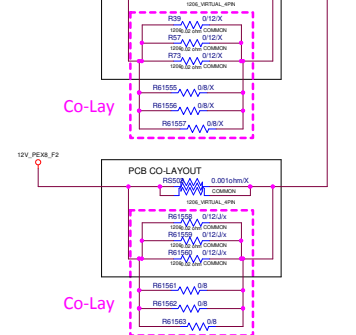
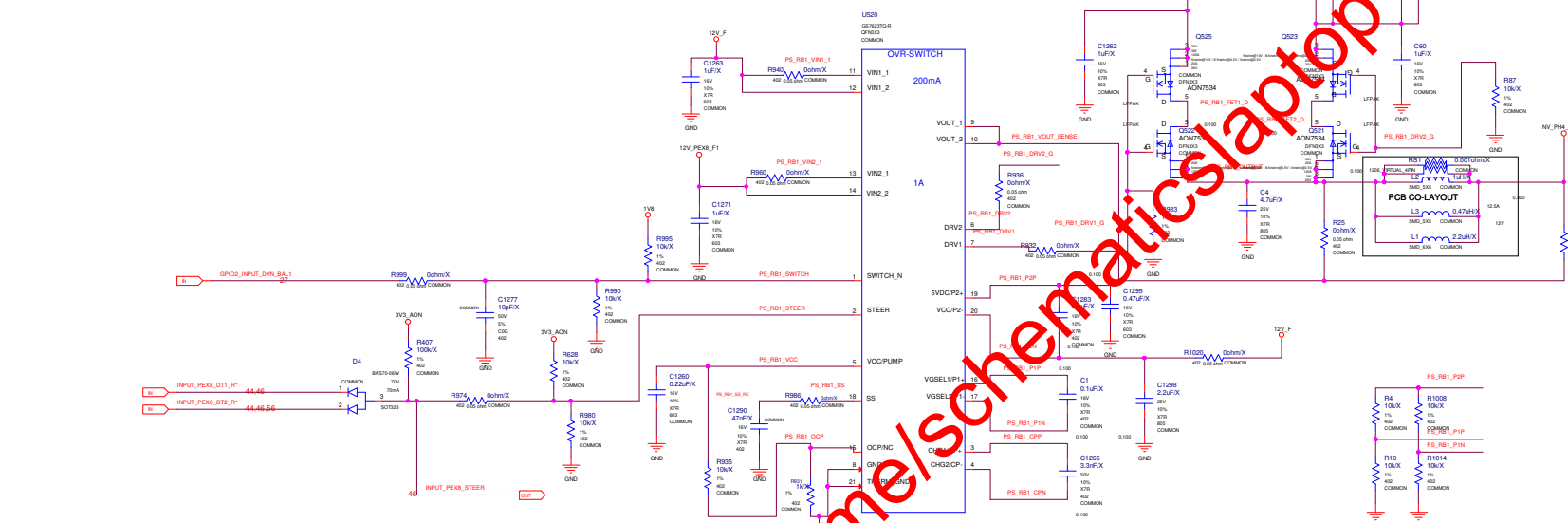


NVVDD PH8b (PWM8b)

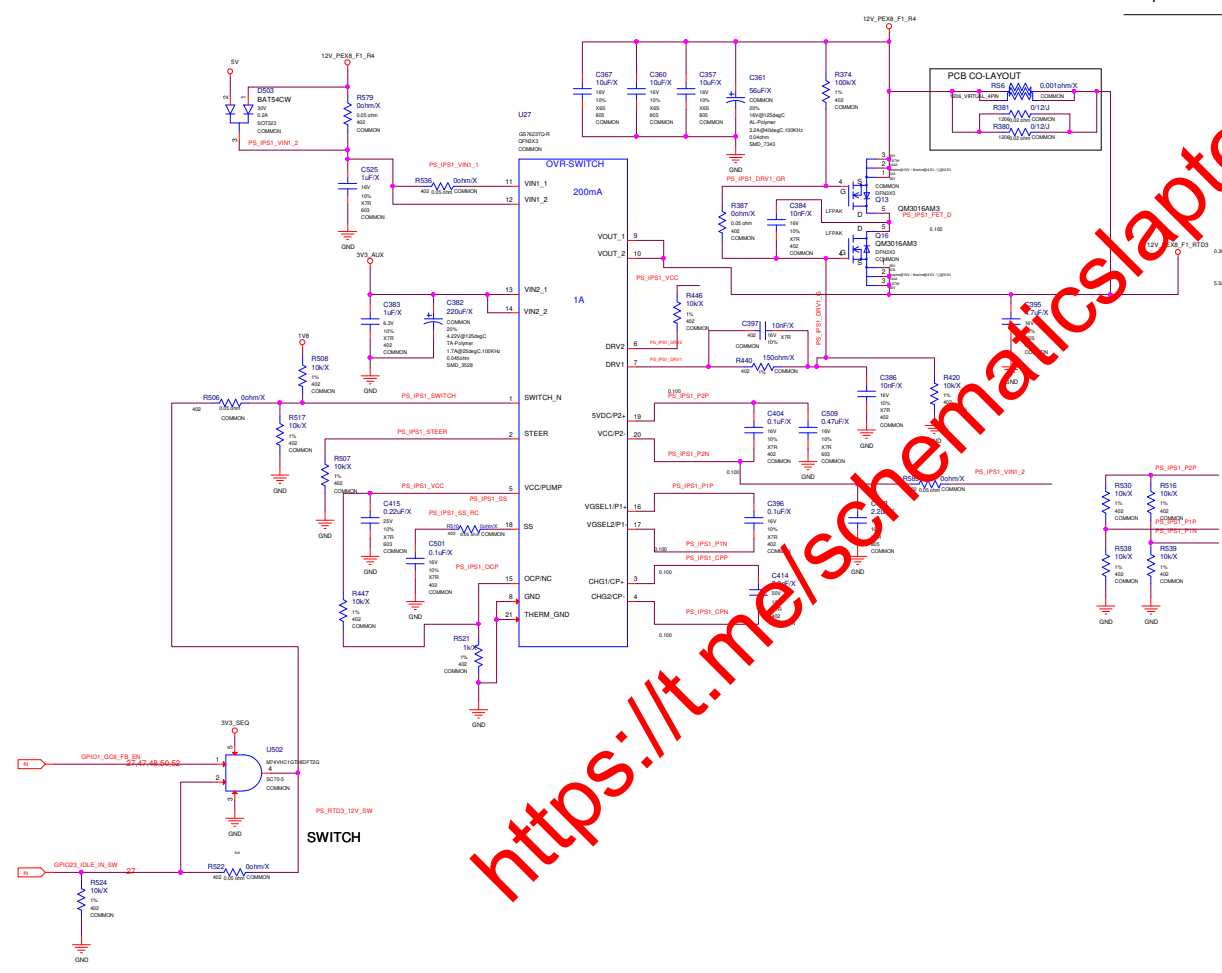




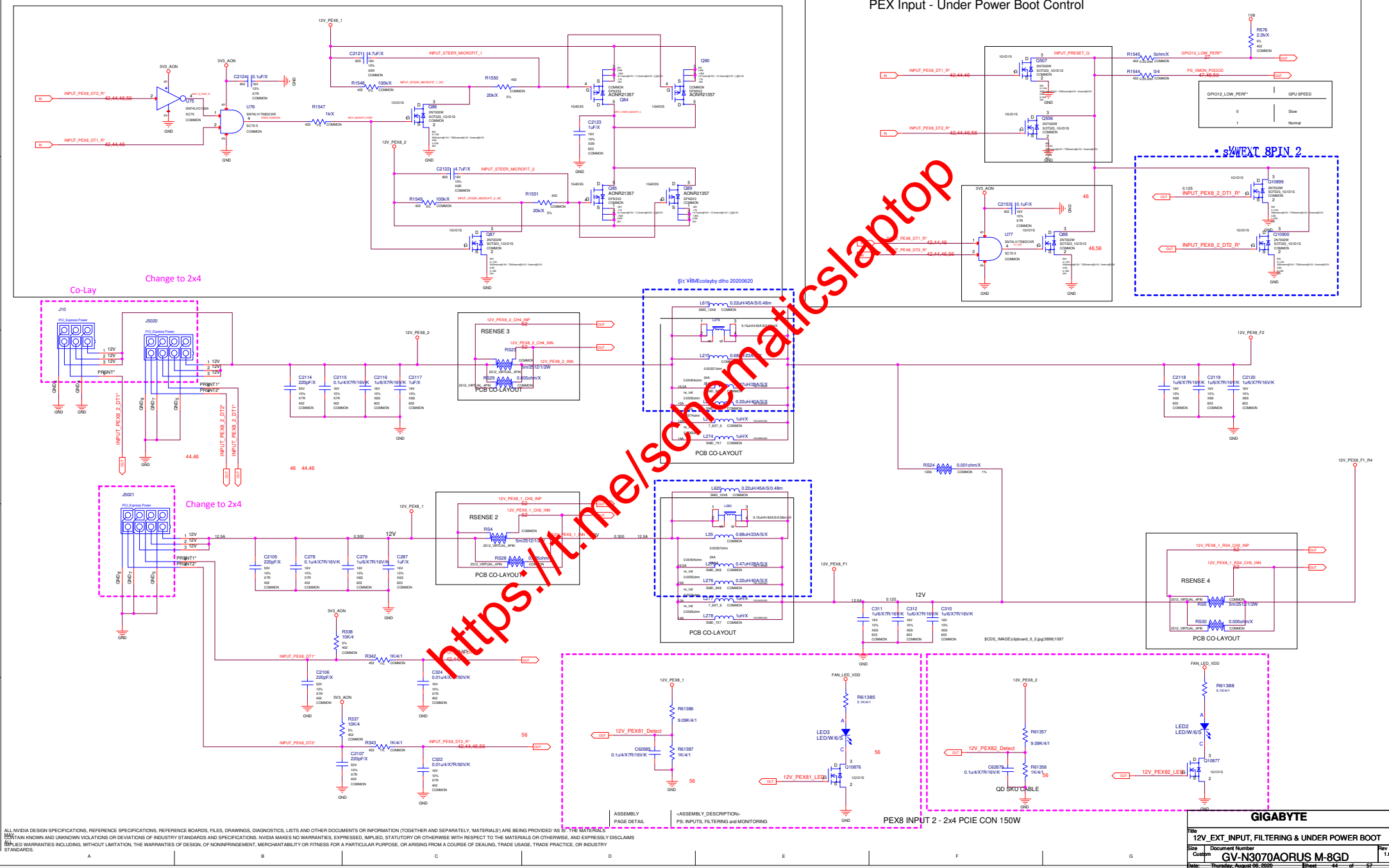


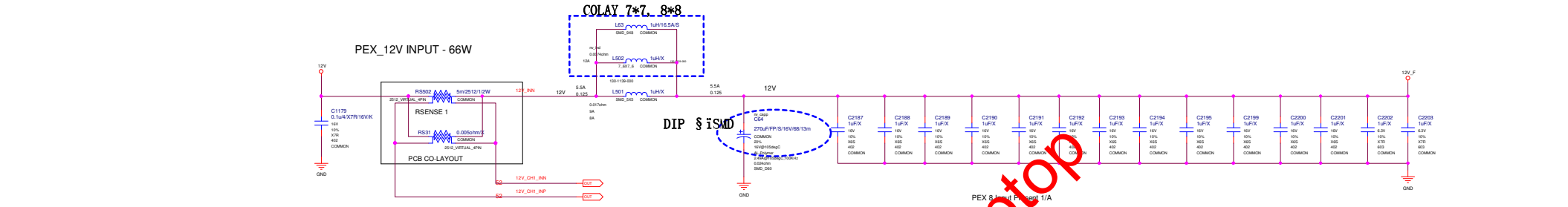


AND GATE LOGIC					
GPIO1	GPIO29	SWITCH	VOUT	SWITCH	VOUT
0	0	0	12V	0	VOUT = VIN1
0	1	0	12V	1	VOUT = VIN2
1	0	0	12V		
1	1	1	3V3A		

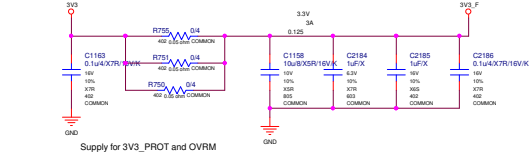


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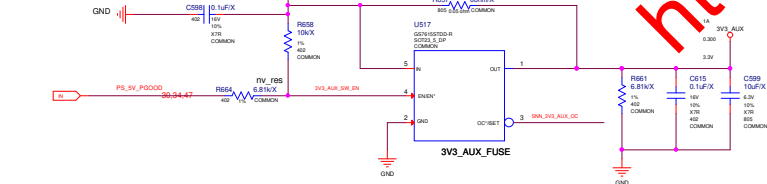




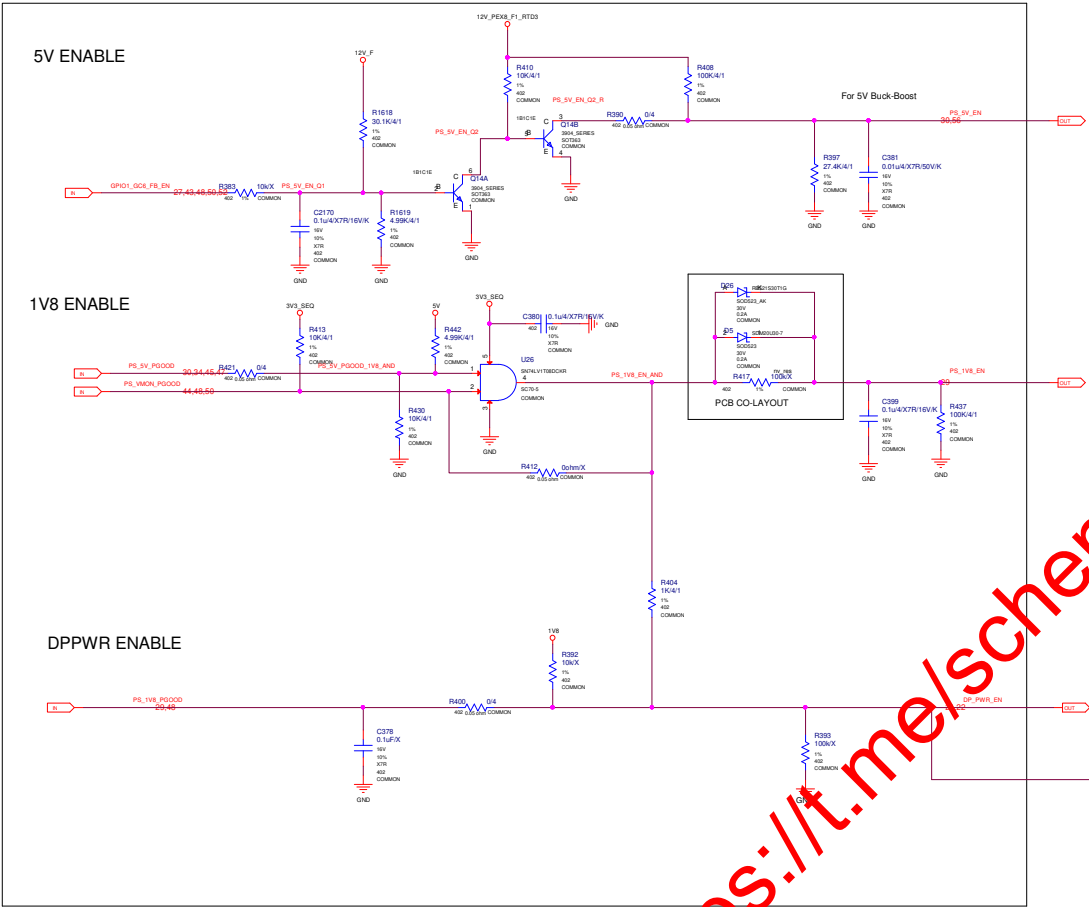
PEX 3V3 INPUT - 10W



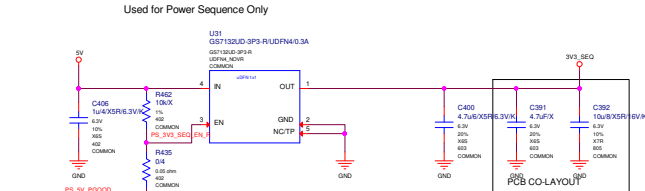
3V3\_AUX



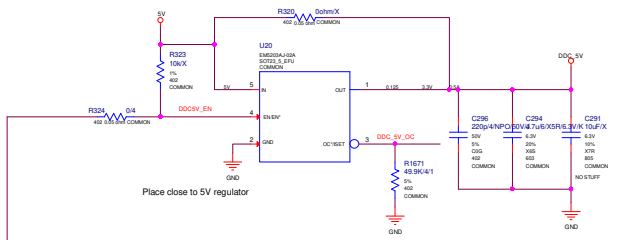




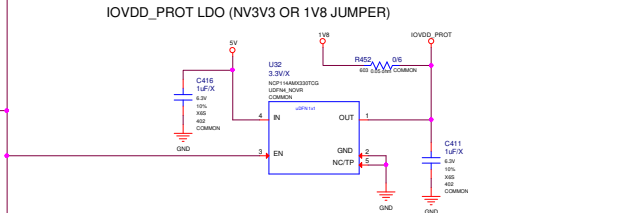
3V3\_SEQ



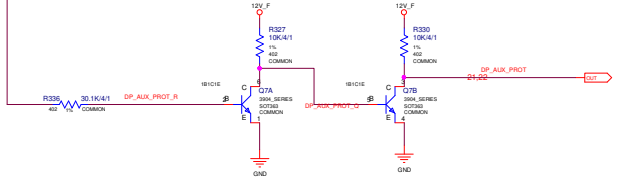
DDC\_5V

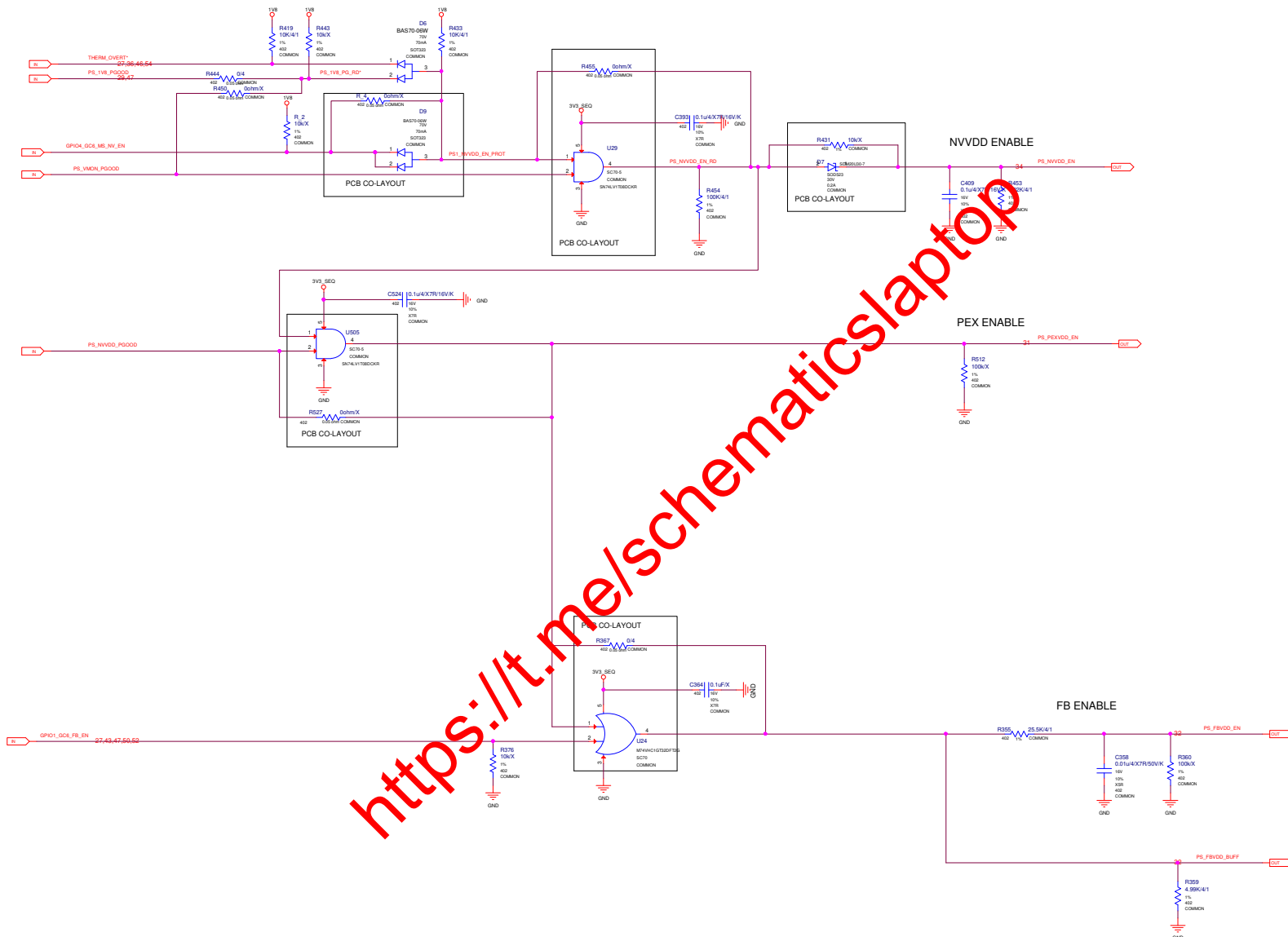


IOVDD\_PROT

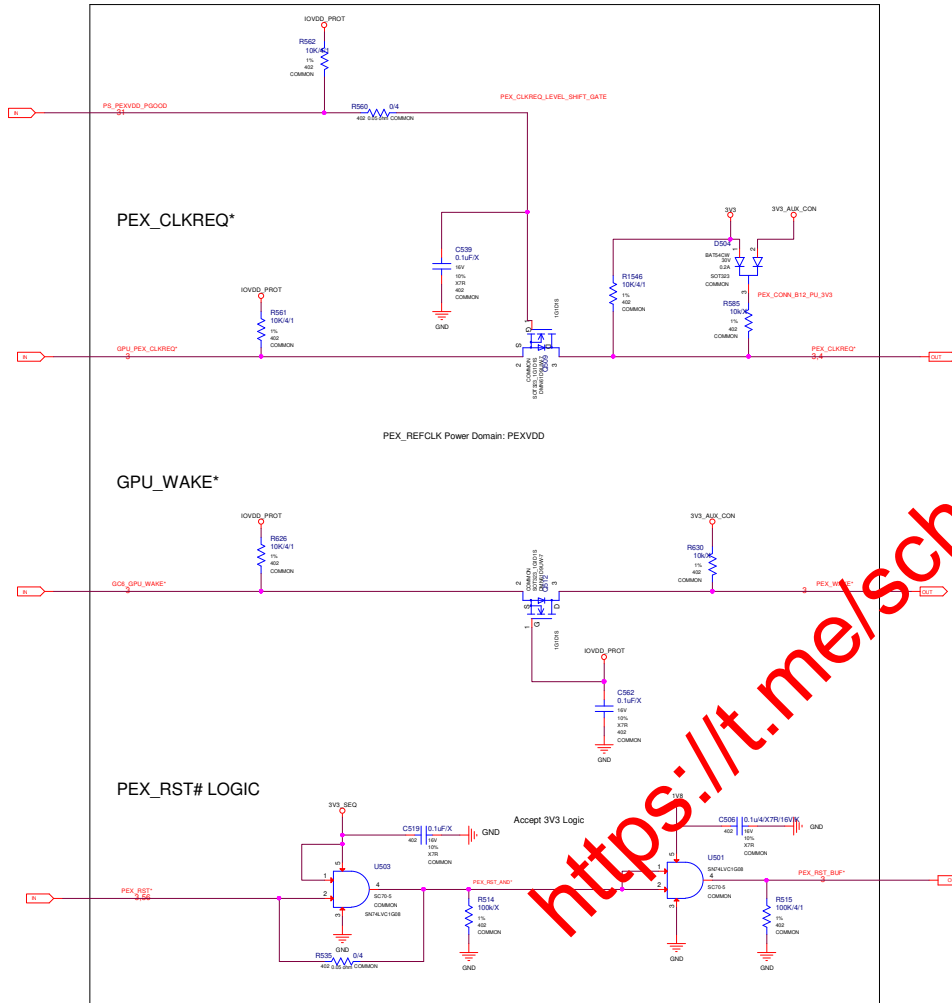


DP\_AUX PROTECTION



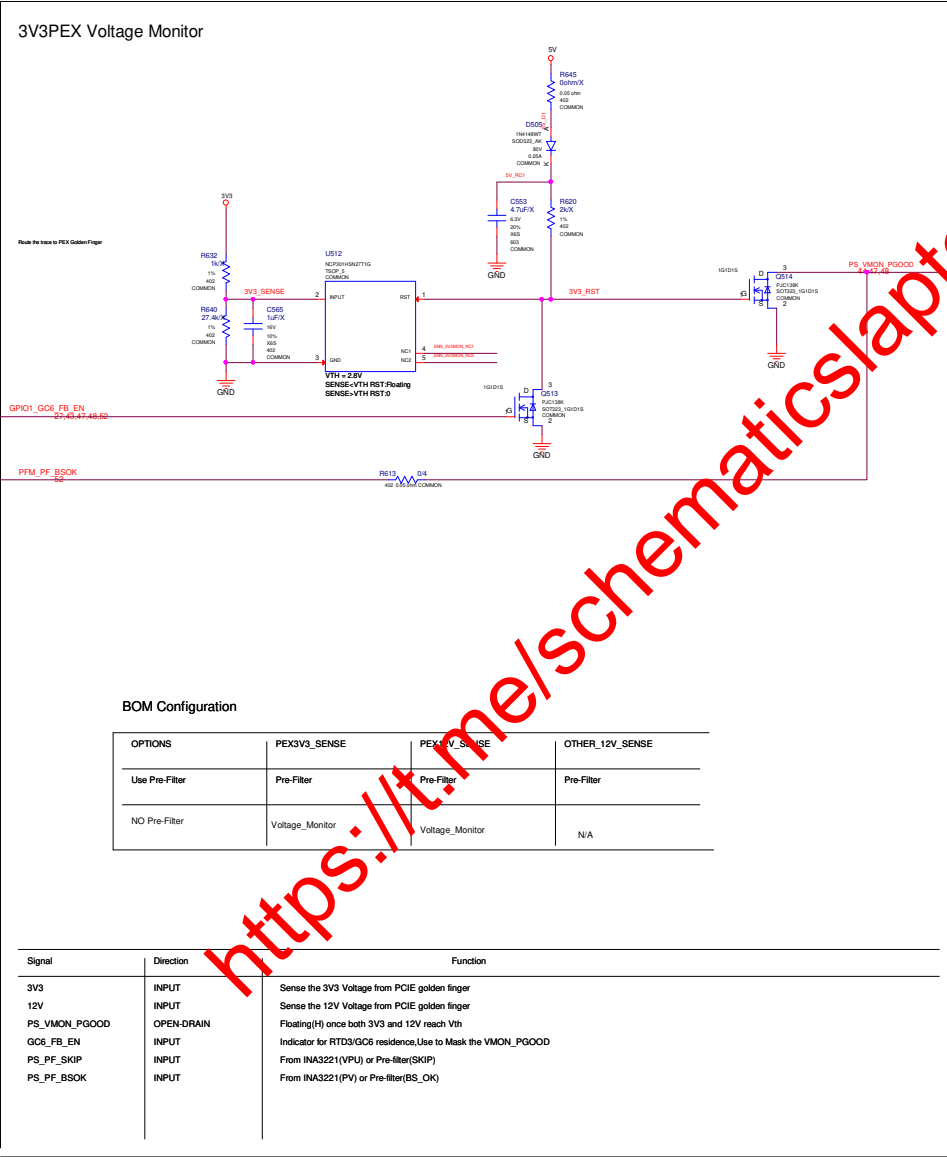


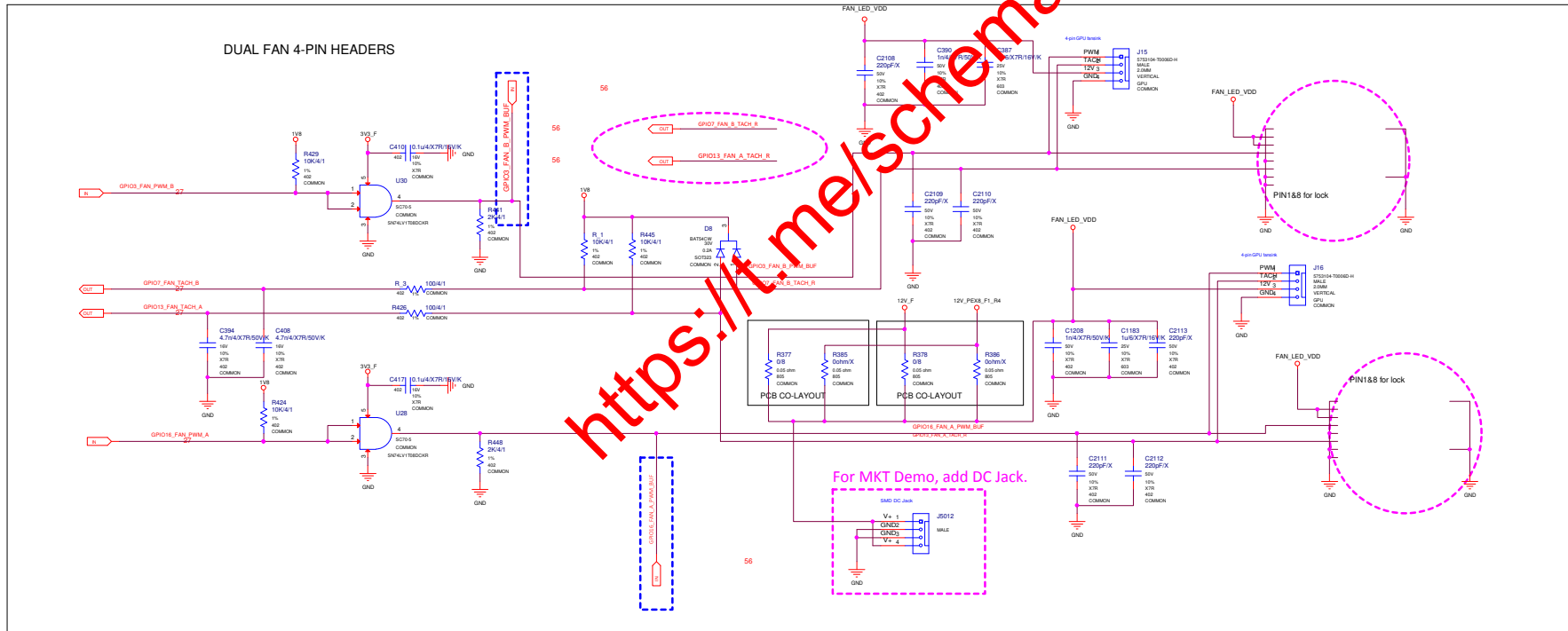




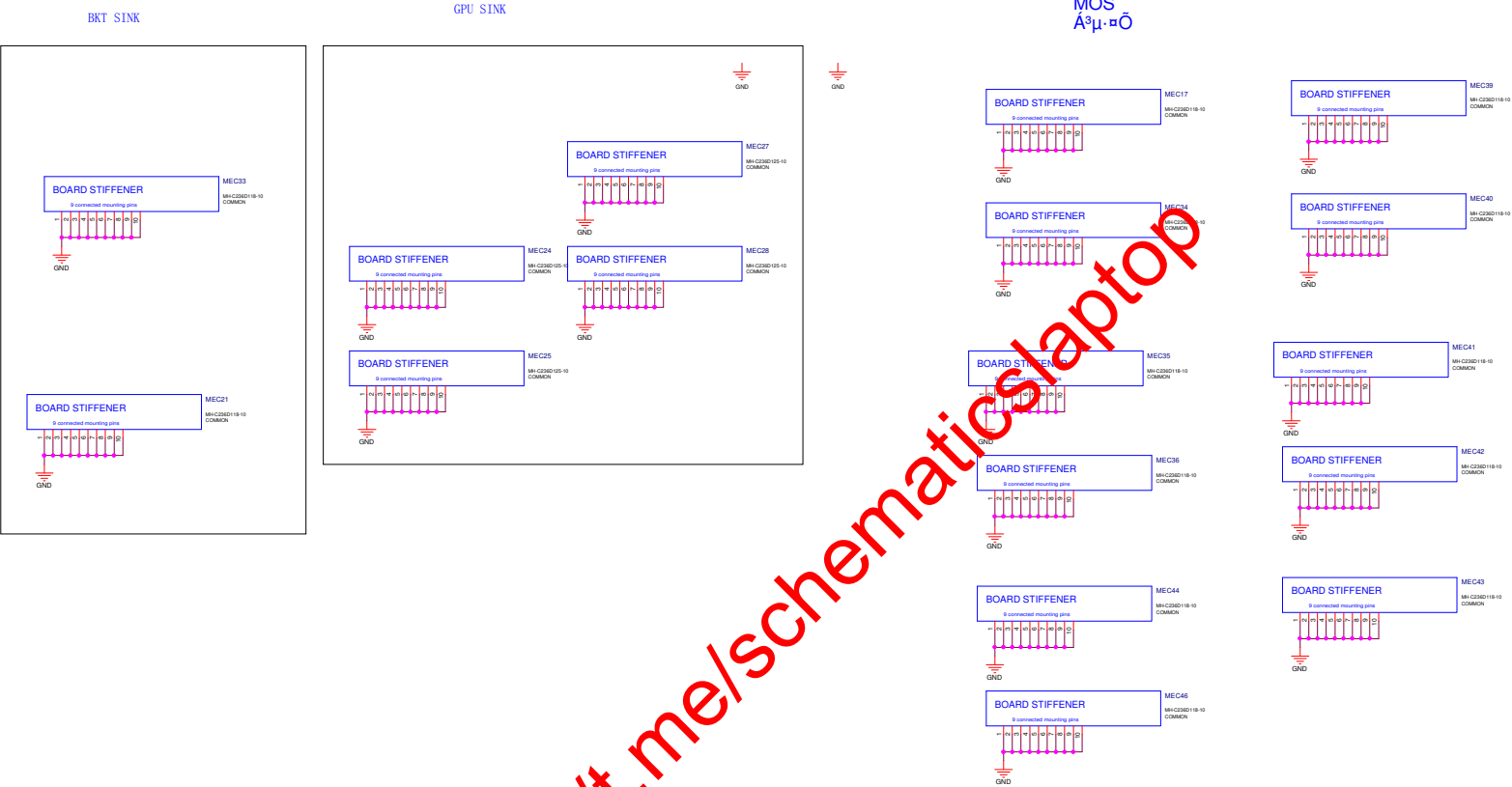
The schematic diagram illustrates the 3V3 logic section of the PEX-8120. Key components include:

- 3V3\_AUX\_CDN**: A node connected to a 3V3 supply through a BAT15W diode and a resistor network (R154E, R156).
- R154E**: A 10K/41 resistor.
- R156**: A 10K/41 resistor.
- R157**: A 10K/41 resistor.
- R158**: A 10K/41 resistor.
- C500**: A 0.1μF/X capacitor.
- 3V3**: The output of the 3V3 logic section.

















History

Date	Modify
2018.07.21	First version

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